

# Mockingbird-N/V/L 14/15\_CML & Hellcat14/15\_CML UMA Schematic

**2019/12/09**

**REV: SC**

**DY : None Installed**  
**UMA: UMA only installed**  
**OPS: DISCRTE OPTIMUS installed**

<Core Design>



**Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Cover Page**

Size  
A4

Document Number

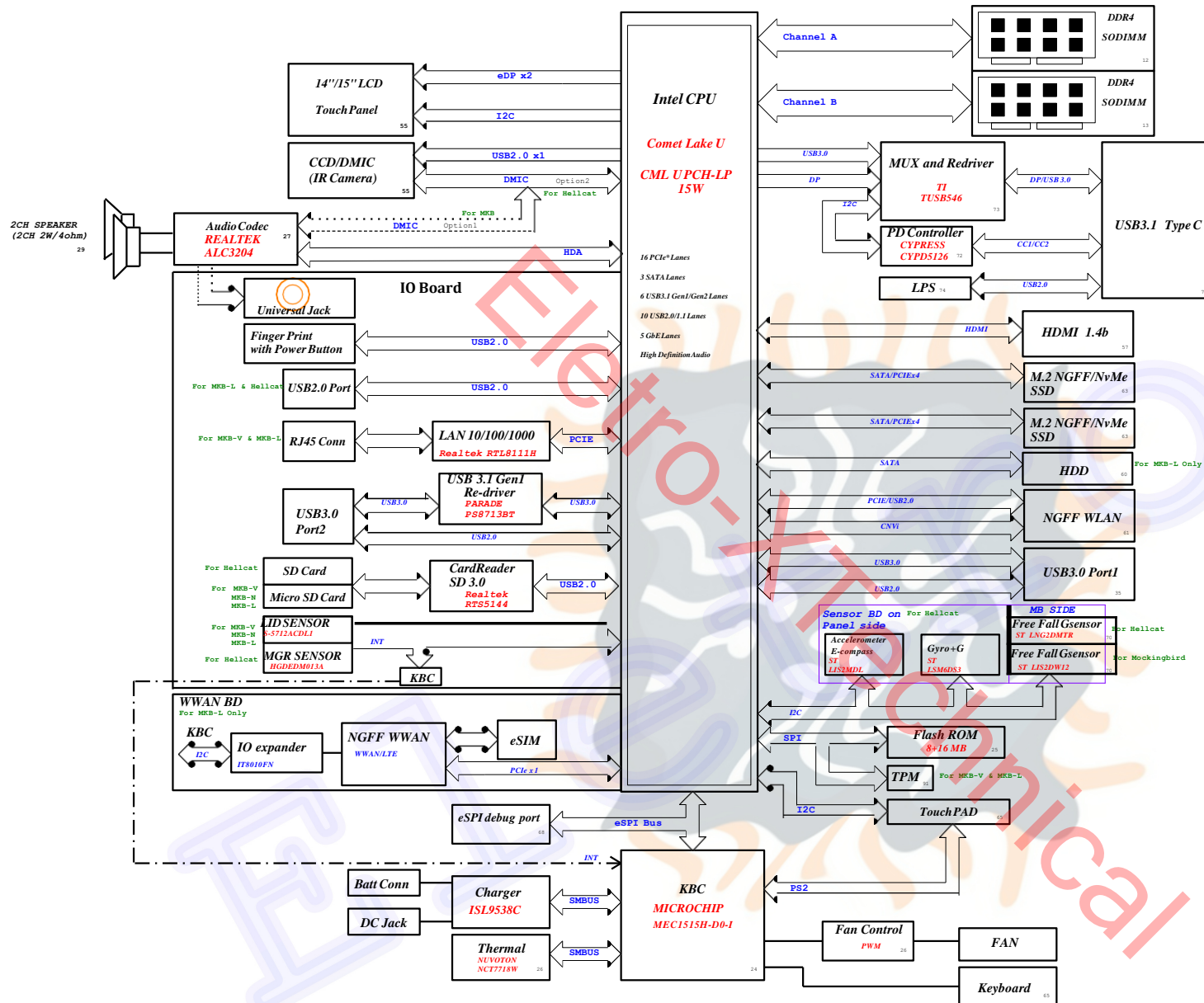
**Mockingbird\_CML**

Date: Monday, December 09, 2019

Sheet 1 of 1

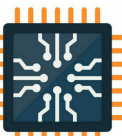


# Mockingbird N/V/L/HellCat CML Block Diagram



Eleto-XTechnical

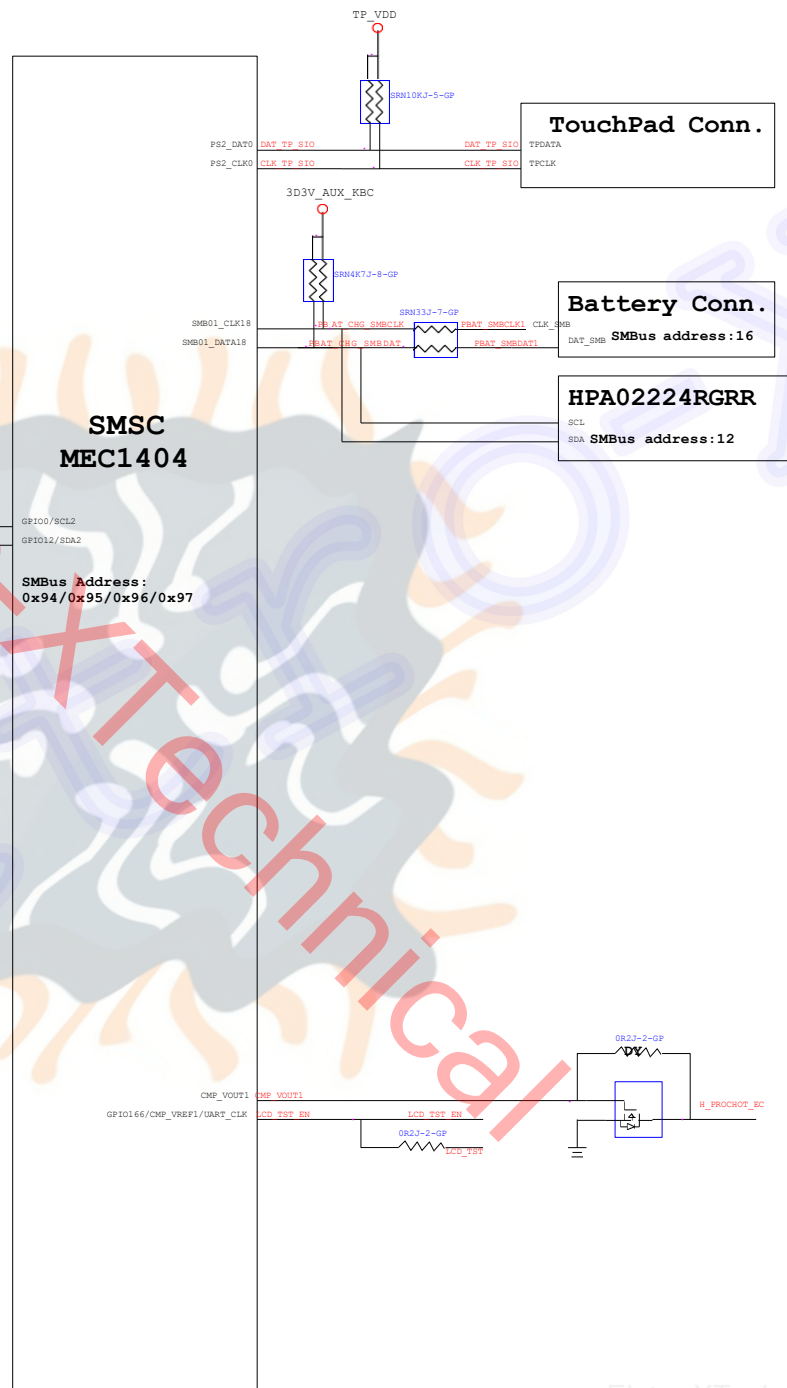
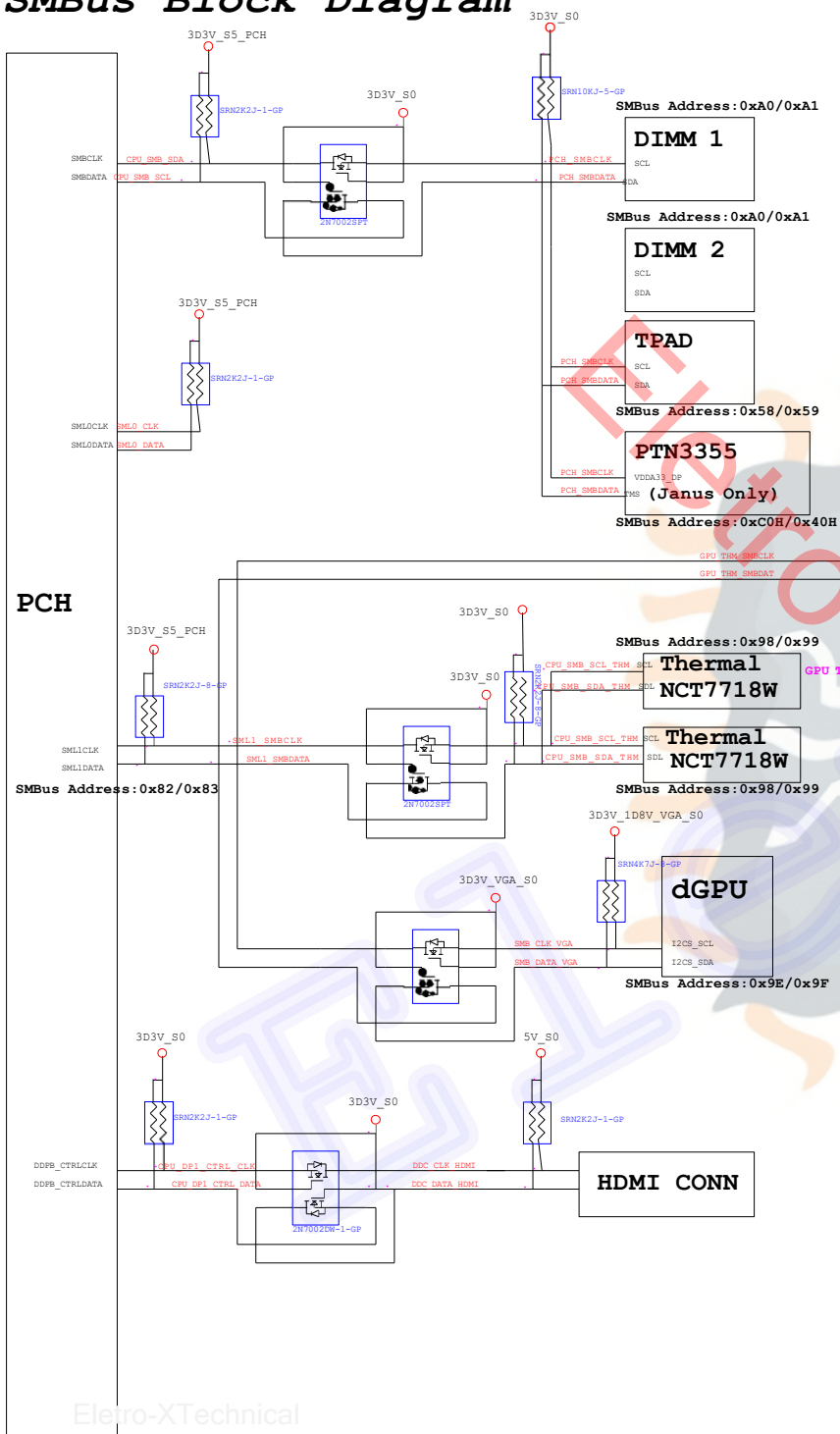
Eleto-XTechnical



# PCH SMBus Block Diagram

# KBC SMBus Block Diagram

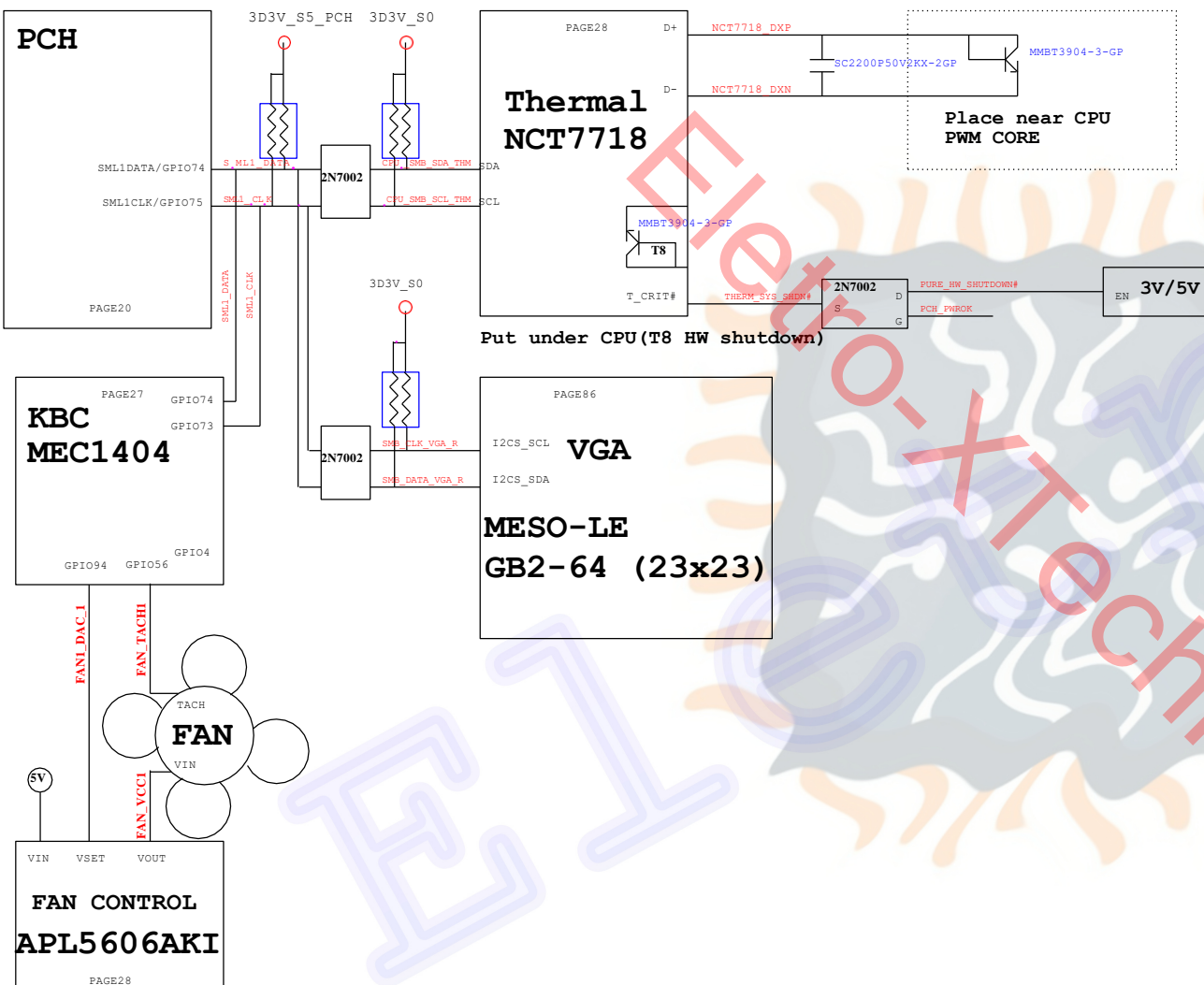
Eletro-XTechnical



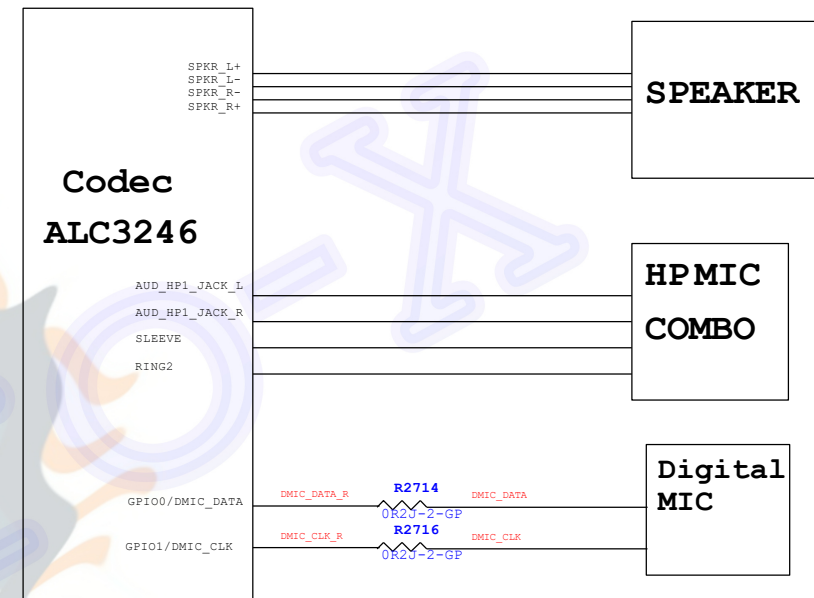
Eletro-XTechnical

Eletro-XTechnical

## Thermal Block Diagram



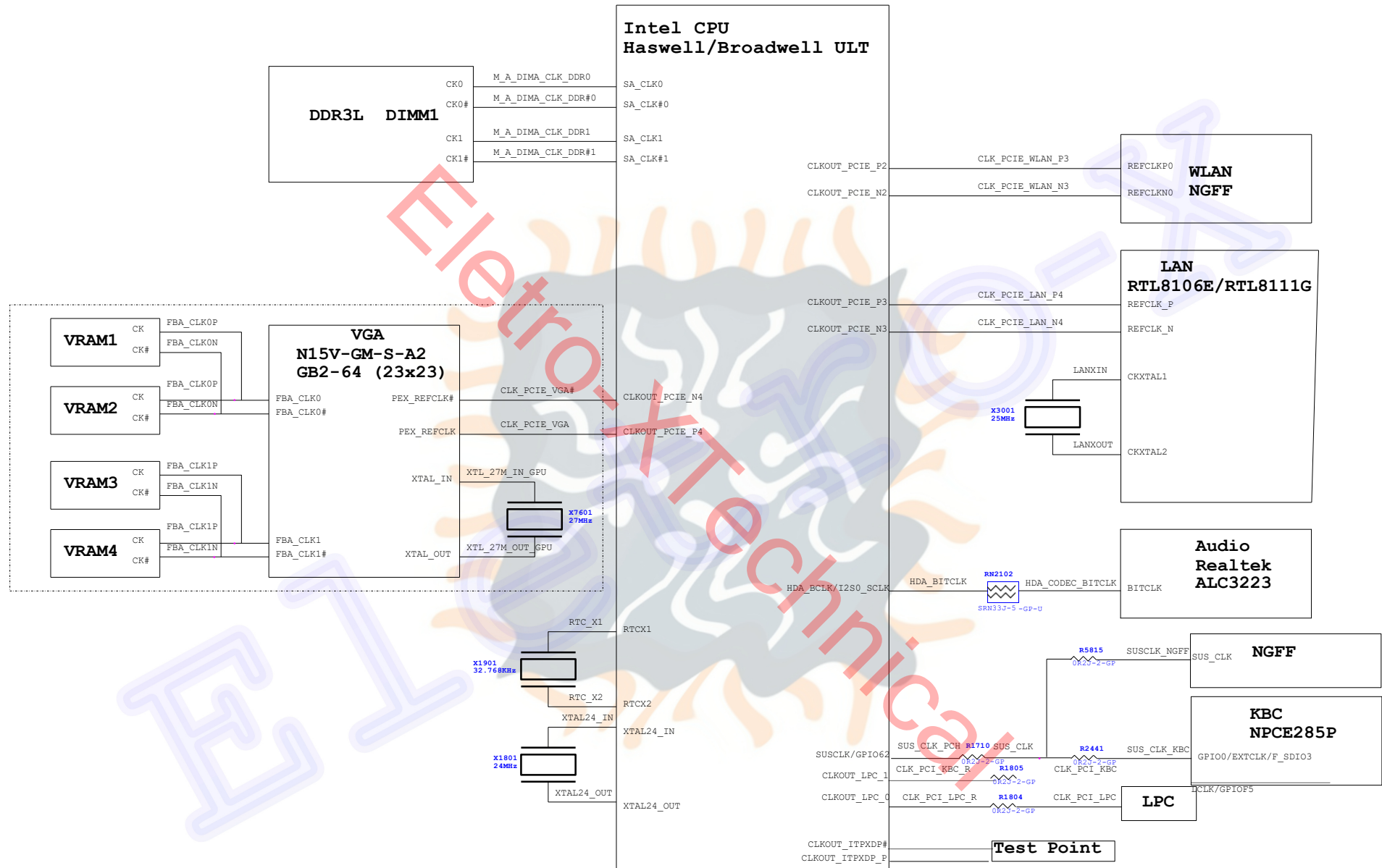
## Audio Block Diagram





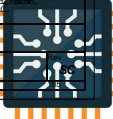
# CLK Block Diagram

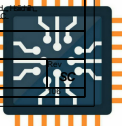
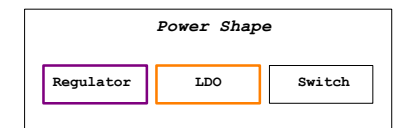
Eletro-XTechnical

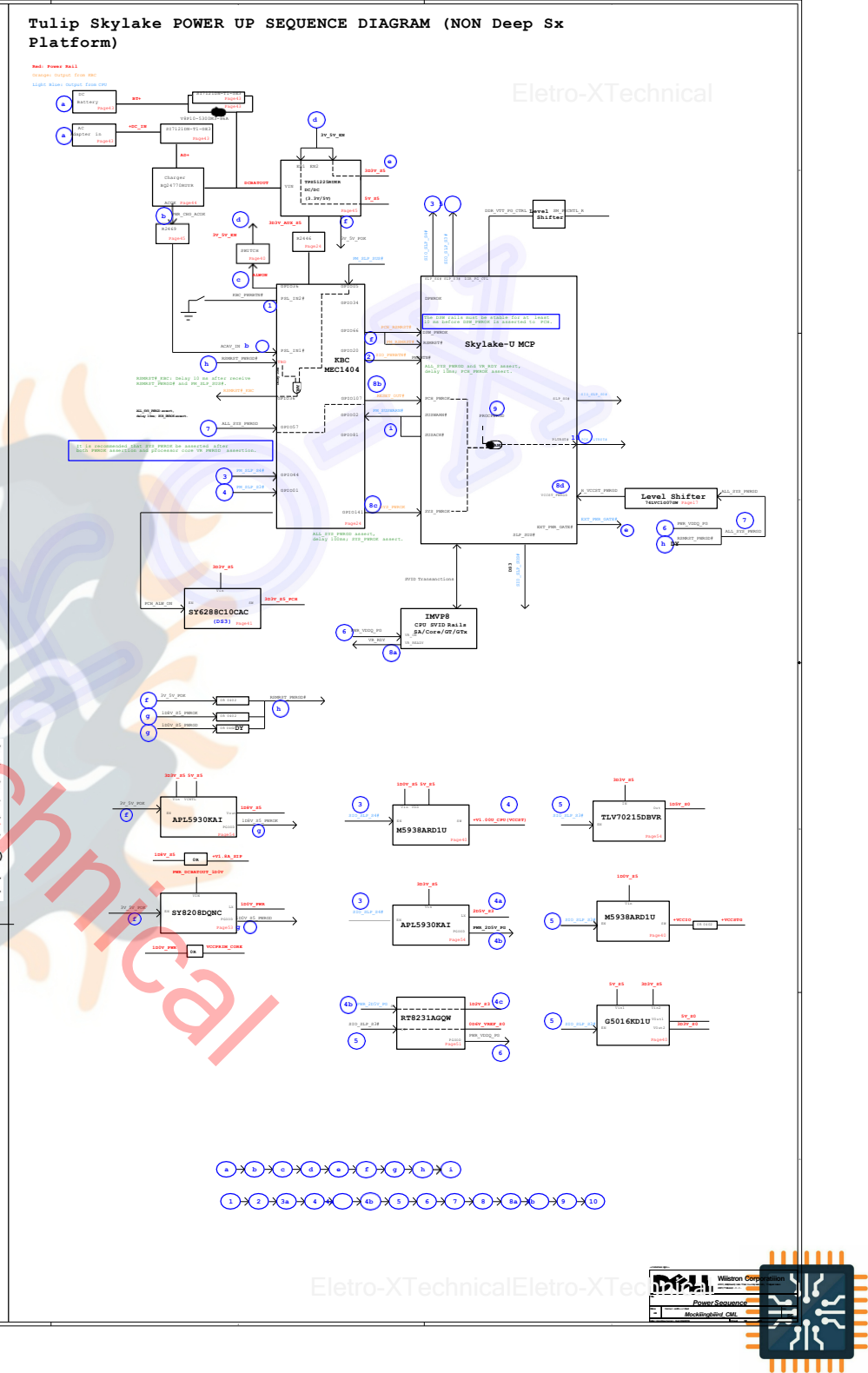
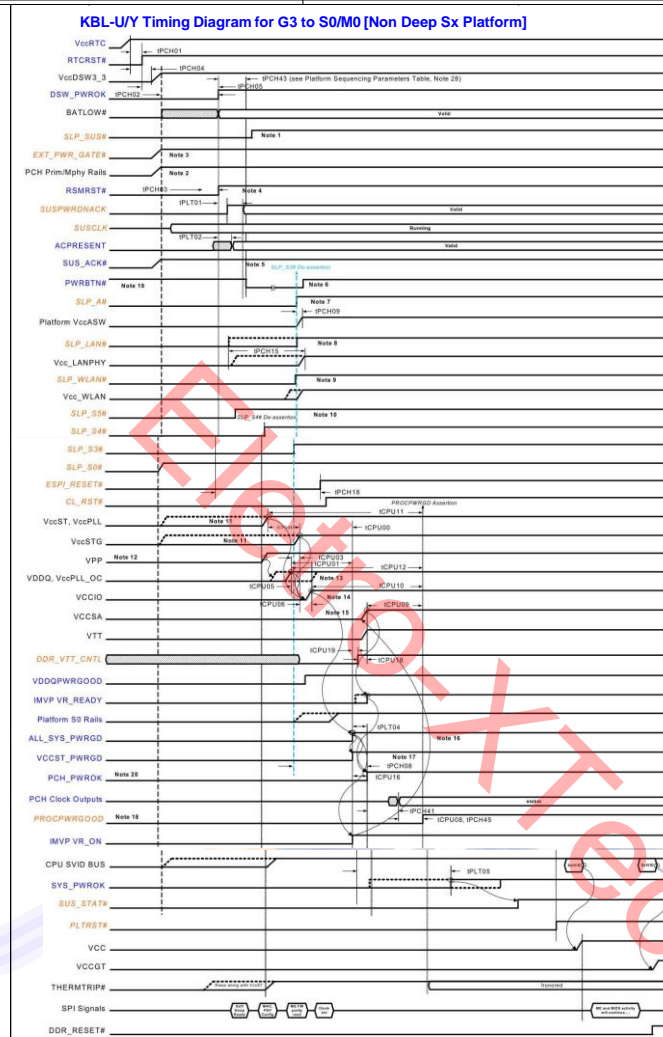
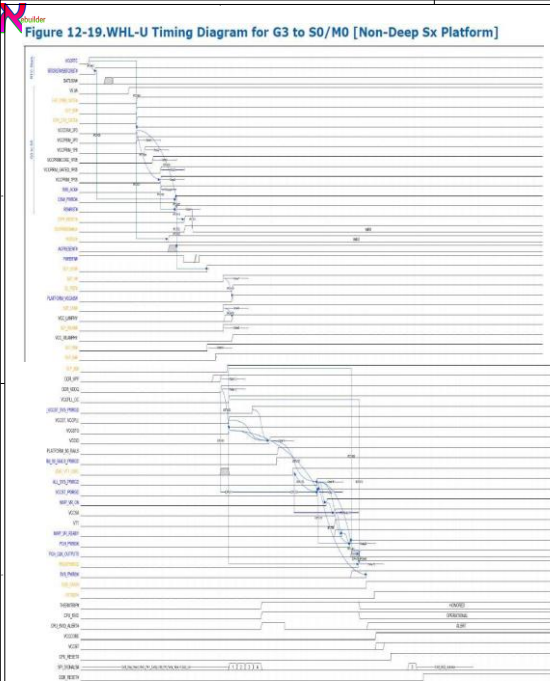


Eletro-XTechnical

Eletro-XTechnical





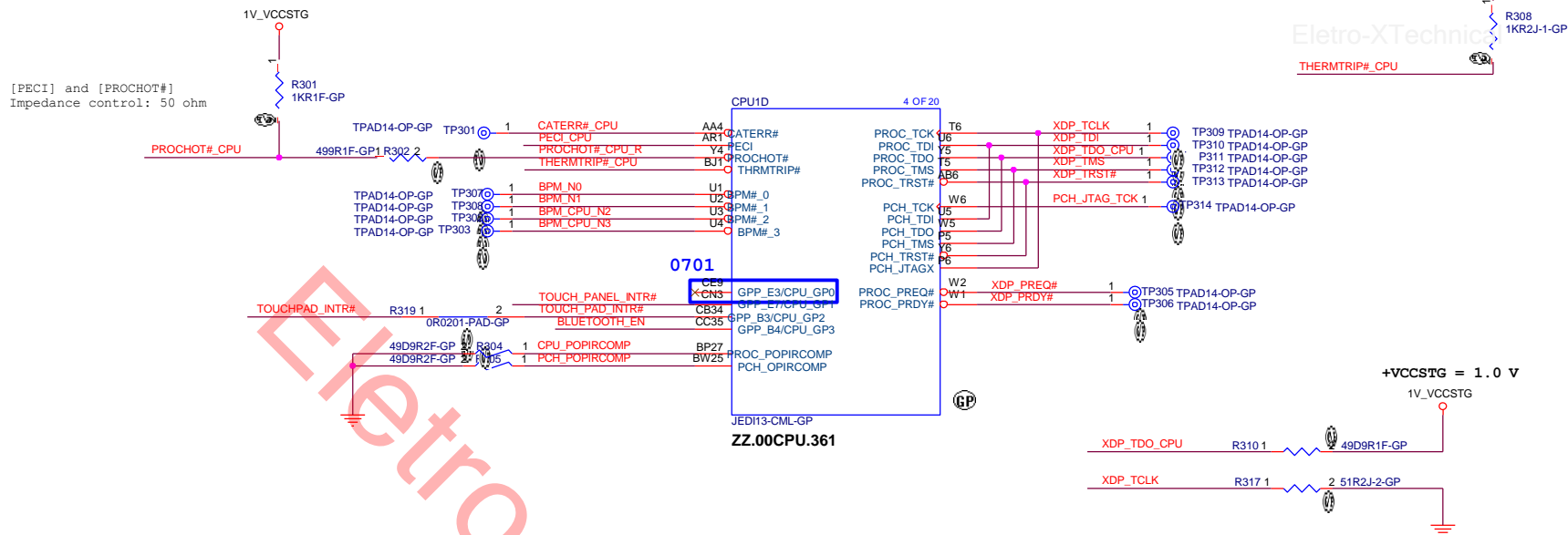


**SSID = CPU**

```

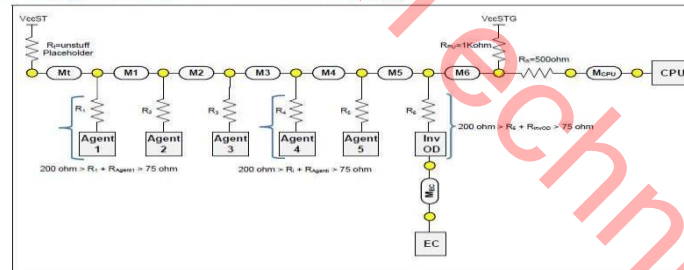
24 PECI_CPU << >> _____
4,46 PROCHOT#_CPU << >> _____
55 TOUCH_PANEL_INTR# << < _____
4,65 TOUCHPAD_INTR# >> > _____
61 BLUETOOTH_EN << < _____

```



(#543016) PROCHOT# Routing

Figure 10-1. Routing Illustration for PROCHOT# Topology

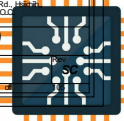


M1,2,3,4,5: <3 inches  
M6: 1-11 inches  
MCPU: 0.3-1.5 inches  
Mt <0.3 mils  
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

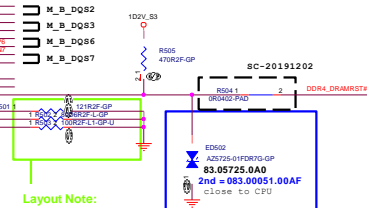
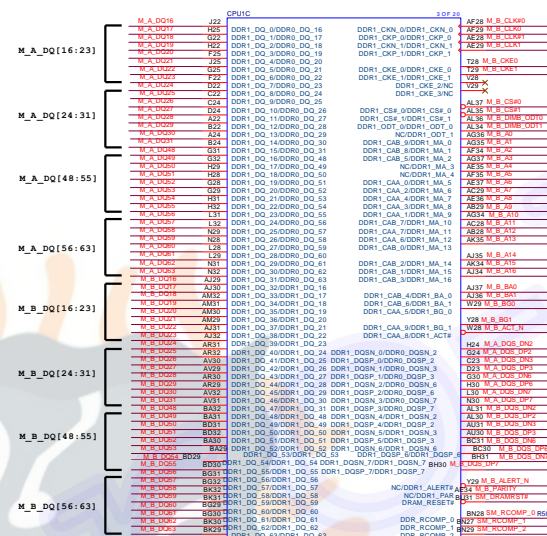
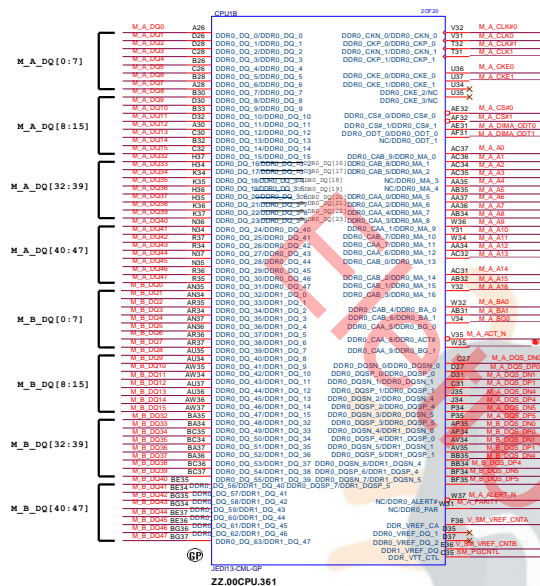
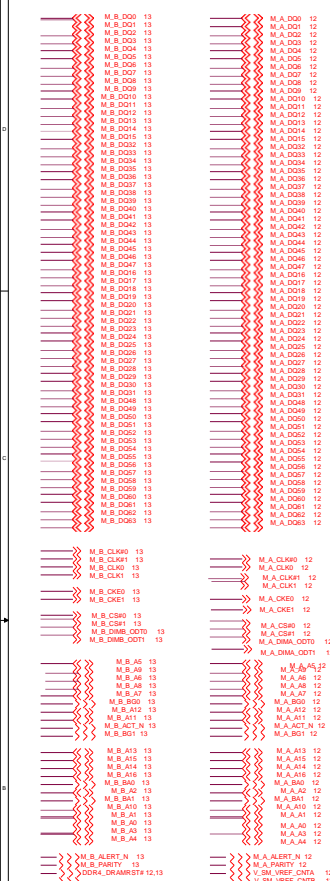


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Title			
CPU (THML/UTAG)			
Size	Document Number		Rev
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DQ Bit Swapping is allowed within the same byte, and Byte Swapping is allowed within the same channel. Clock (CLK and CLK#) and Strobe (DS0 and DS0#) differential signal swapping within a pair is not allowed. Also differential clock pair to clock pair swapping within a channel is not allowed.

PDG: DDR/ODT

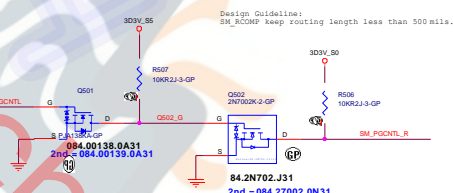
### 4.3 ODT Connectivity

### Table 4-19. ODT Signals Connectivity Table

Processor	Memory type	Side	Signal	Rule
WHL-U	<b>DDR4 Memory Down</b>	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[0] connected to DRAMs' Rank0 ODT. Processor's ODT[1] connected to DRAMs' Rank1 ODT balls. If Rank1 not used Processor ODT[1] not connected.
		DRAMs	ODT[1:0]	
	<b>DDR4 SODIMM</b>	Processor	DDR0_ODT[1:0] DDR1_ODT[1:0]	Processor's ODT[1:0] balls connected to DIMM ODT[1:0] balls.
		DIMMs	ODT[1:0]	

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.

1. For additional ODT signal connection details reference the Customer Reference Board (CRB) schematics and board files.



Design Guideline:

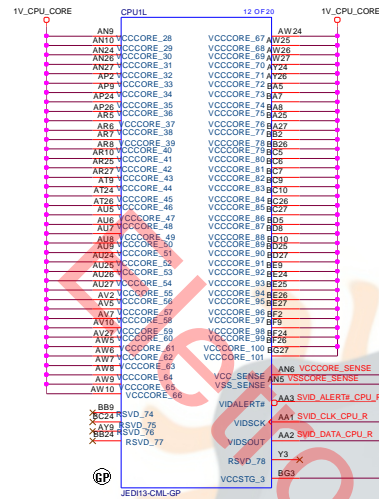
### Layout Note

0614 Layout H7





46 VCCORE\_SENSE <<<====  
46 VSSCORE\_SENSE <<<====  
46 SVID\_DATA\_CPU <<<====  
46 SVID\_CLK\_CPU <<<====  
46 SVID\_ALERTt\_CPU <<<====



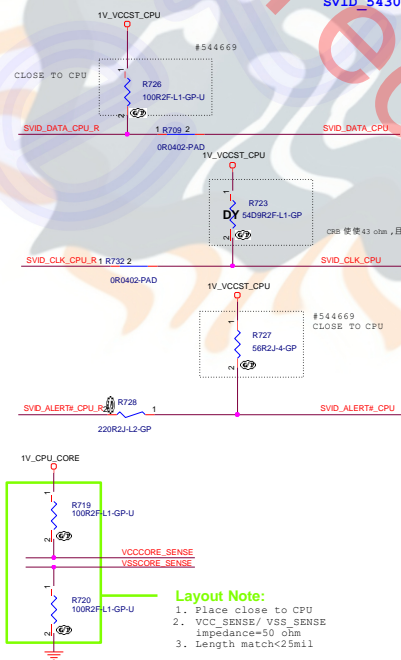
Layout Note:  
The total Length of Data and Clock (from CPU to each VR) must be equal (10.1 inch).  
Route the Alert signal between the Clock and the Data signals.

SVID 543016:

### SVID DATA

### SVID CLOCK

### SVID ALERT



Layout Note:  
1. Place close to CPU  
2. VCC\_SENSE/ VSS\_SENSE  
impedance=50 ohm  
3. Length match<25mil

Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M1	MS/SL/DSL	VSS		76	76	2992.13	2992.13
Segment	Line Type	Reference	Via Count	Max Length, mm		Max Length, Mils	
				Segment	Total	Segment	Total
M2	MS/SL/DSL	VSS		381		15000	
M3	MS/SL/DSL	VSS		102	432	4015.75	17007.9
M4	MS/SL/DSL	VSS		102		4015.75	
M5	MS/SL/DSL	VSS		102		4015.75	
M6	MS/SL/DSL	VSS		3	3	118.11	118.11
M7	MS/SL/DSL	VSS		3	3	118.11	118.11
M8	MS/SL/DSL	VSS		3	3	118.11	118.11
M9	MS/SL/DSL	VSS		3	3	118.11	118.11
M10	MS/SL/DSL	VSS		3	3	118.11	118.11
M11	MS/SL/DSL	VSS		3	3	118.11	118.11
M12	MS/SL/DSL	VSS		3	3	118.11	118.11
M13	MS/SL/DSL	VSS		3	3	118.11	118.11

**Topology Guidelines**

SVID Signals: VIDSOUT, VIDSCK, VIDSALERT#

VIDSOUT platform resistors: Rpu1=1000, Rpu2=1000, Rr1=00, Rr2=100

VIDSCK platform resistors: Rpu1=Empty, Rpu2=450, Rr1=00, Rr2=49.90

VIDSALERT# platform resistors: Rpu1=560, Rpu2=Empty, Rr1=2200, Rr2=00

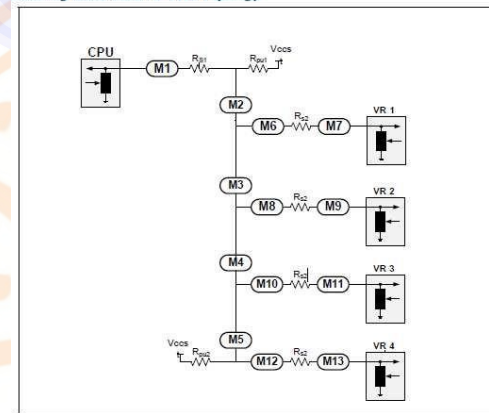
Platform resistors tolerances: ± 5%

Route ordering: When routing at minimum spacing route Alert between Data and Clock

**Length Matching Rules**

Length Matching between VIDSOUT and VIDSCK: ± 100mils

#### Routing Illustration for SVID Topology



Core Design

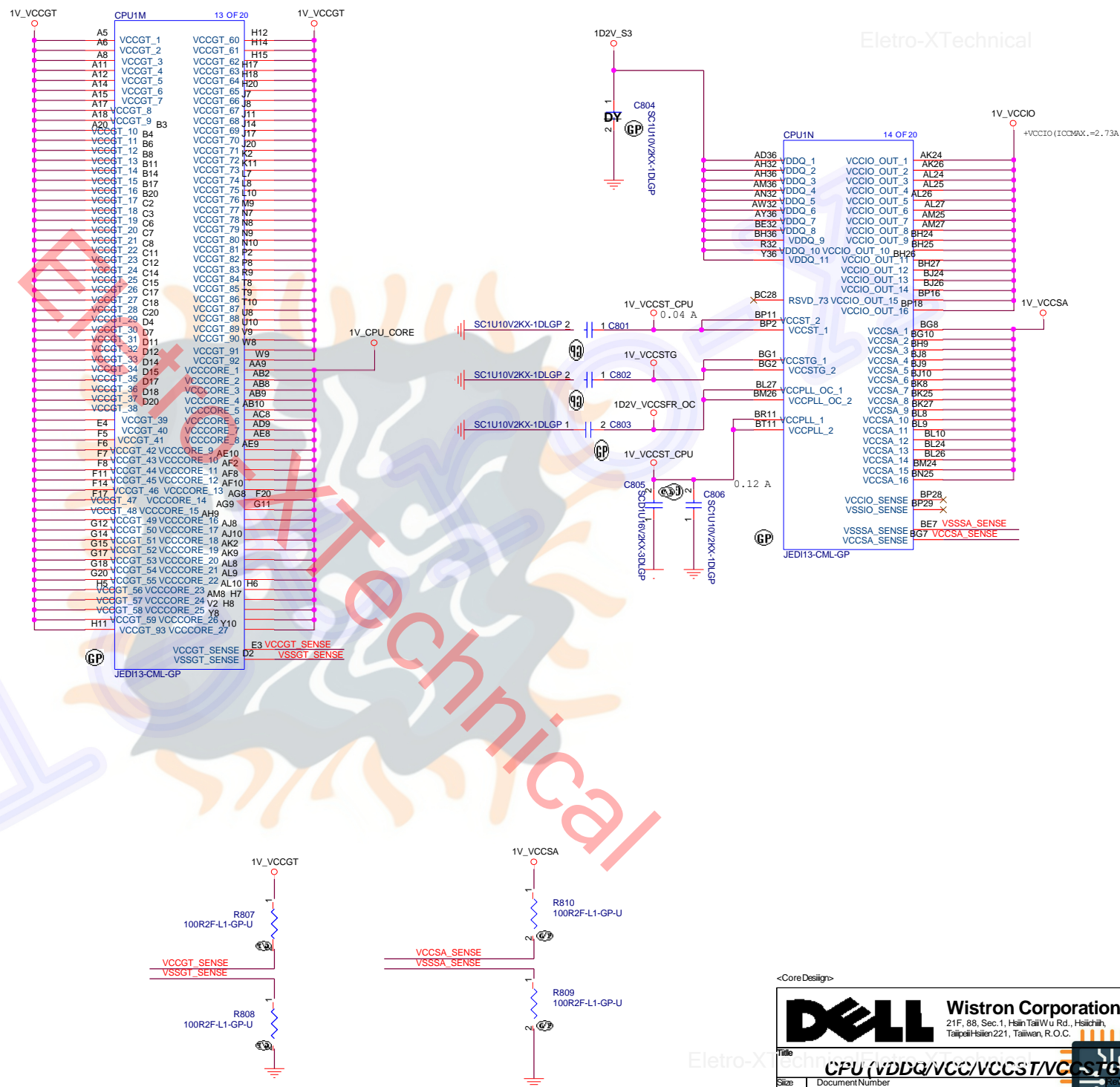
**Wistron Corporation**

**CPU (VCCIN/VID)**

**Mockingbird\_CML**

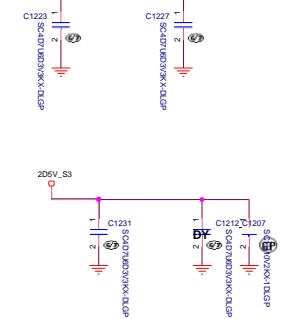
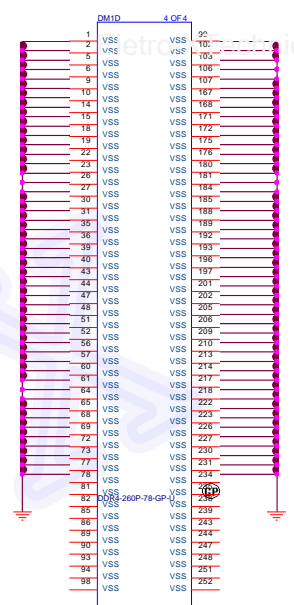
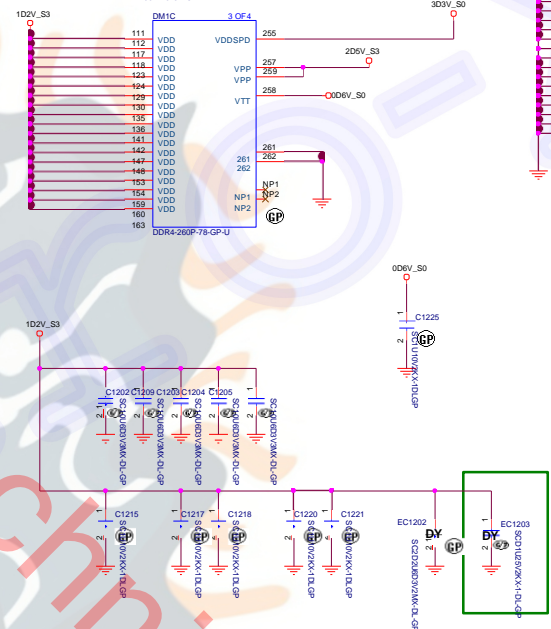
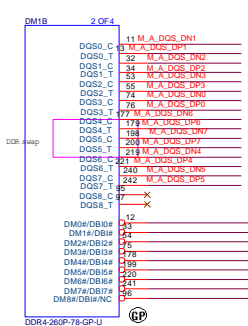
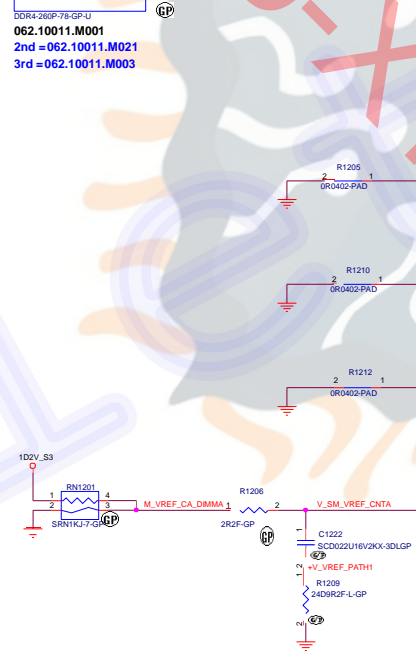
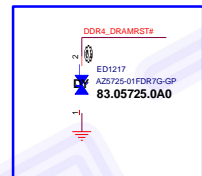
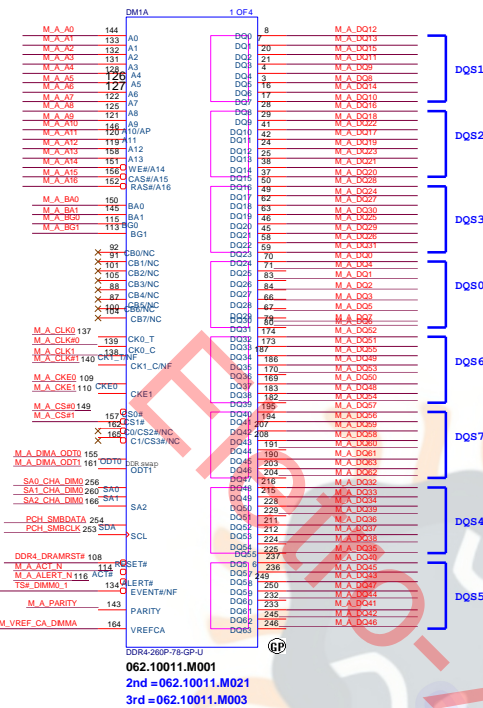
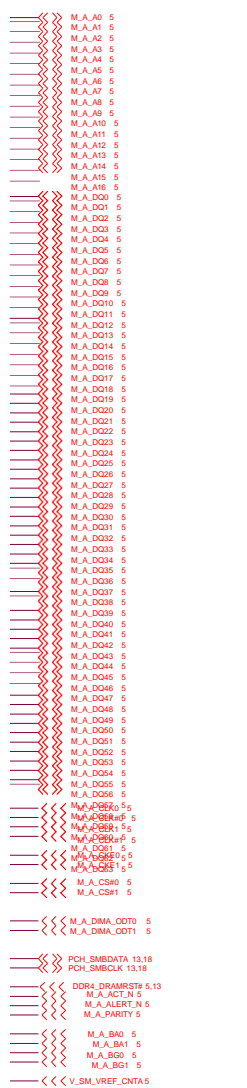
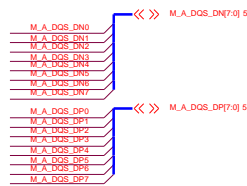
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Document Number: Mockingbird\_CML  
Date: Monday, December 09, 2015  
Sheet: 7

# Eletro-X





SSID = MEMORY







#543014:  
220 pF nominal capacitors are recommended for Gen 3.  
100 pF nominal capacitors are recommended for Gen 2.

#543059: The xHCI controller supports USB Debug port on all USB3.0 capable ports.

Eletro-XTechnical



COLAY WITH:  
8 PCB RESISTORS ON CPU SIDE

SSD2

HDD1

SSD1

Layout Note:  
1. Power Width: 4 mils min (maximum) 12-15 mils (trace)  
2. Isolation Spacing: At least 12 mils to any adjacent high speed I/O

#543016: When used as DEVSLP, no external pull-up or pull-down termination required from SATA Host DEVSLP.

#543011: The SATA2SD signal is open-collector and requires a weak external pull-up (8.2 kΩ to 10 kΩ) to Vcc1\_3.

Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
High Speed I/O (HSIO) Type and Lane	USB3.1 Gen1/Gen2 #1	USB3.1 Gen1/Gen2 #2	USB3.1 Gen1/Gen2 #3	USB3.1 Gen1/Gen2 #4	USB3.1 Gen1/Gen2 #5	USB3.1 Gen1/Gen2 #6	PCIe* #7	PCIe* #8	PCIe* #9	PCIe* #10	PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16
Intel® RST Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

Table 1-3. PCH HSIO Detail

SKU	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Mainstream/Base-U	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	USB 3.1 Gen 1	PCIe*	PCIe*	GbE OA/PCIe*	GbE OB/PCIe*	GbE OC/PCIe*	PCIe*	SATA 0/PCIe*	SATA 1A/PCIe*	GbE OD/PCIe*	GbE OE/PCIe*	PCIe*	PCIe*
Premium-U	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	GbE OA/PCIe*	GbE OB/PCIe*	GbE OC/PCIe*	PCIe*	PCIe*/SATA 0	PCIe*/SATA 1A	GbE OD/PCIe*	GbE OE/PCIe*	PCIe*/SATA 1B	PCIe*/SATA 2
Premium-Y	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	PCIe*/USB 3.1 Gen 1	GbE OA/PCIe*	GbE OB/PCIe*	GbE OC/PCIe*	PCIe*	PCIe*/SATA 0	PCIe*/SATA 1A	GbE OD/PCIe*	GbE OE/PCIe*	Not Available	Not Available

Table 24-2. PCI Express® Port Feature Details

SKL	Max Device (Ports)	Max Lanes	PCIe* Gen Type	Encoding	Transfer Rate (MT/s)	Theoretical Max Bandwidth (GB/s)		
						x1	x2	x4
U	6	12	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00
			3	128b/130b	8000	1.00	2.00	3.94
Y	5	10	1	8b/10b	2500	0.25	0.50	1.00
			2	8b/10b	5000	0.50	1.00	2.00

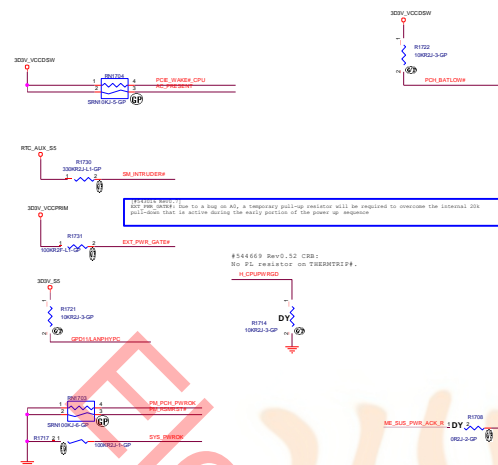
PCH-LP	PCIe* Controller #1	PCIe* Controller #2	PCIe* Controller #3	PCIe* Controller #4	Flex I/O Lane															
					0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Premium-U	RP1	RP2	RP3	RP4	RP5				RP6				RP7				RP8			
					RP9				RP10				RP11				RP12			
					RP13				RP14				RP15				RP16			
					RP17				RP18				RP19				RP20			

Eletro-XTechnical

Eletro-XTechnical

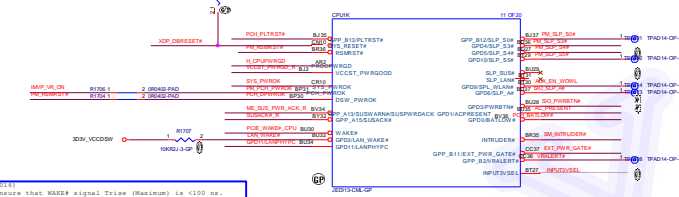
Eletro-X





```
#544669 Rev0.32 CBB:
No PL resistor on TRESNTRIP#.
H_CUPWINGD
```

WAKE#: Ensure that WAKE# signal Trise (Maximum) is <100 ns.

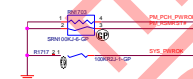


**External Pull-up requirement for SLP\_S0# and EXT\_PWR\_GATE# signal pins**

SLP\_S0# and EXT\_PWR\_GATE# signal pins require External Pull-up and the details are given below:

Signal Name	Pull-up Resistor Value		Note
	3.3V Signaling Mode	1.8V Signaling Mode	
EXT_PWR_GATE#	500k	75k	Pull-up resistor is required
SLP_S0#	500k	75k	Pull-up resistor is required if a device is monitoring SLP_S0# before RSP0# for

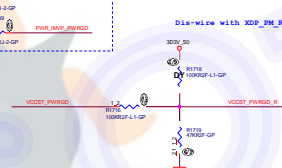
BATLOW#:  
Pull-up required even if not implemented.



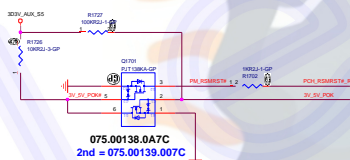
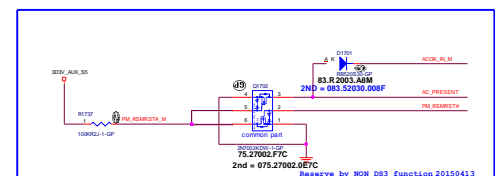
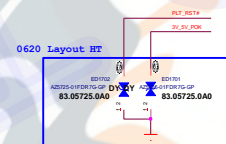
AOZ Power switch, P/N: 074.01334.0093  
Low Rds(on) = 5m Ohm  
Turn on rise time = 10us



20190424(EVT)  
Reverse R1705, R1739 by Dell Andy  
R1705  
PWRJMP\_PWRGO: 1 DY 100% ON

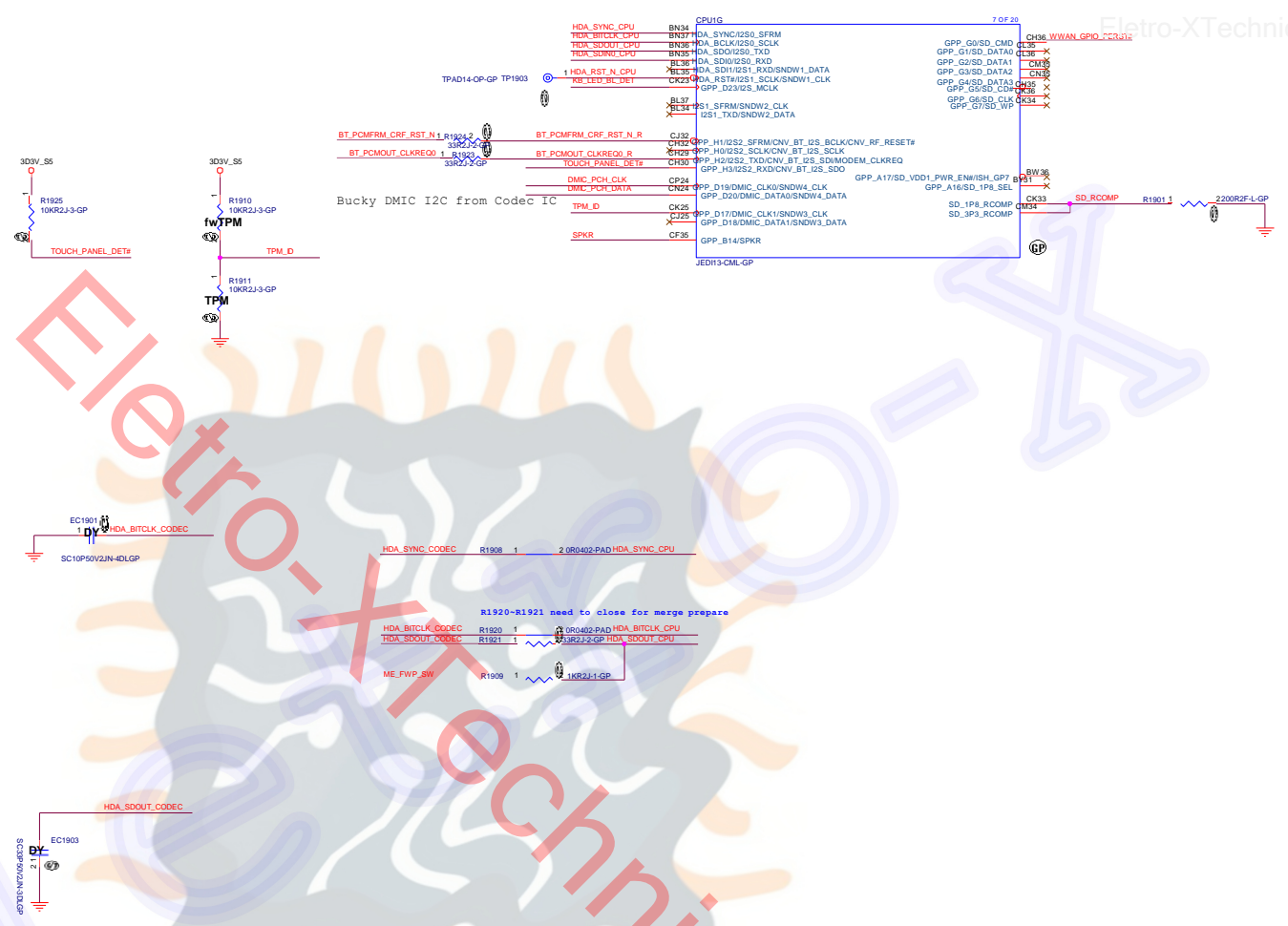
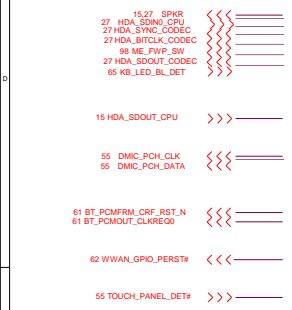


R1722 & EC1708 modify to 100k and 0.01uF at DVT1

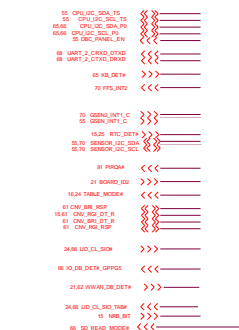




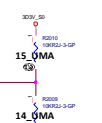
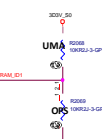
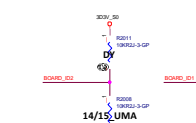
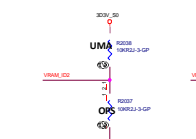
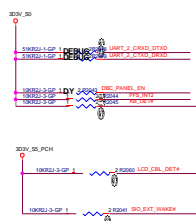




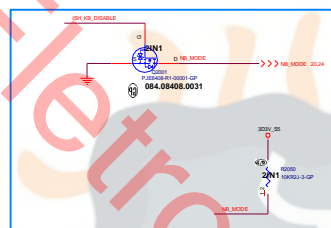
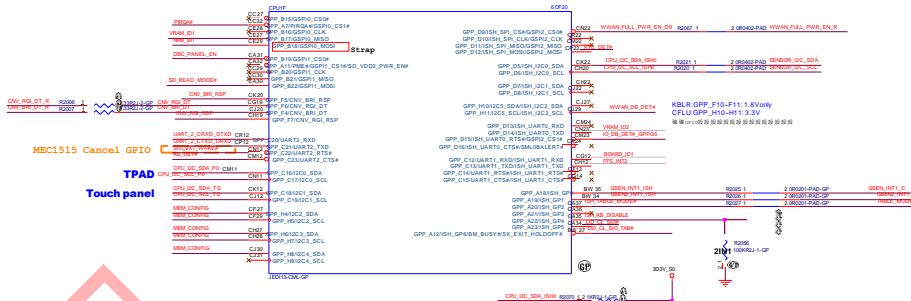




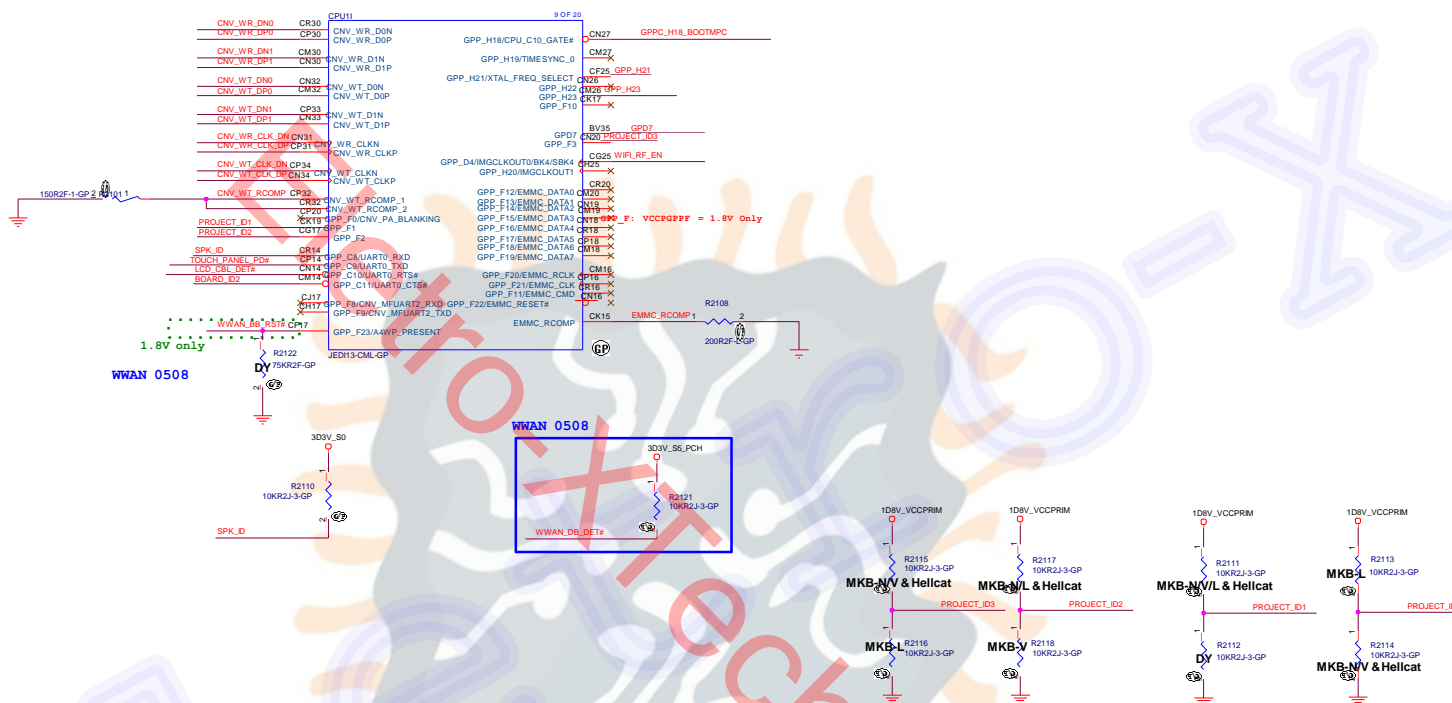
0513



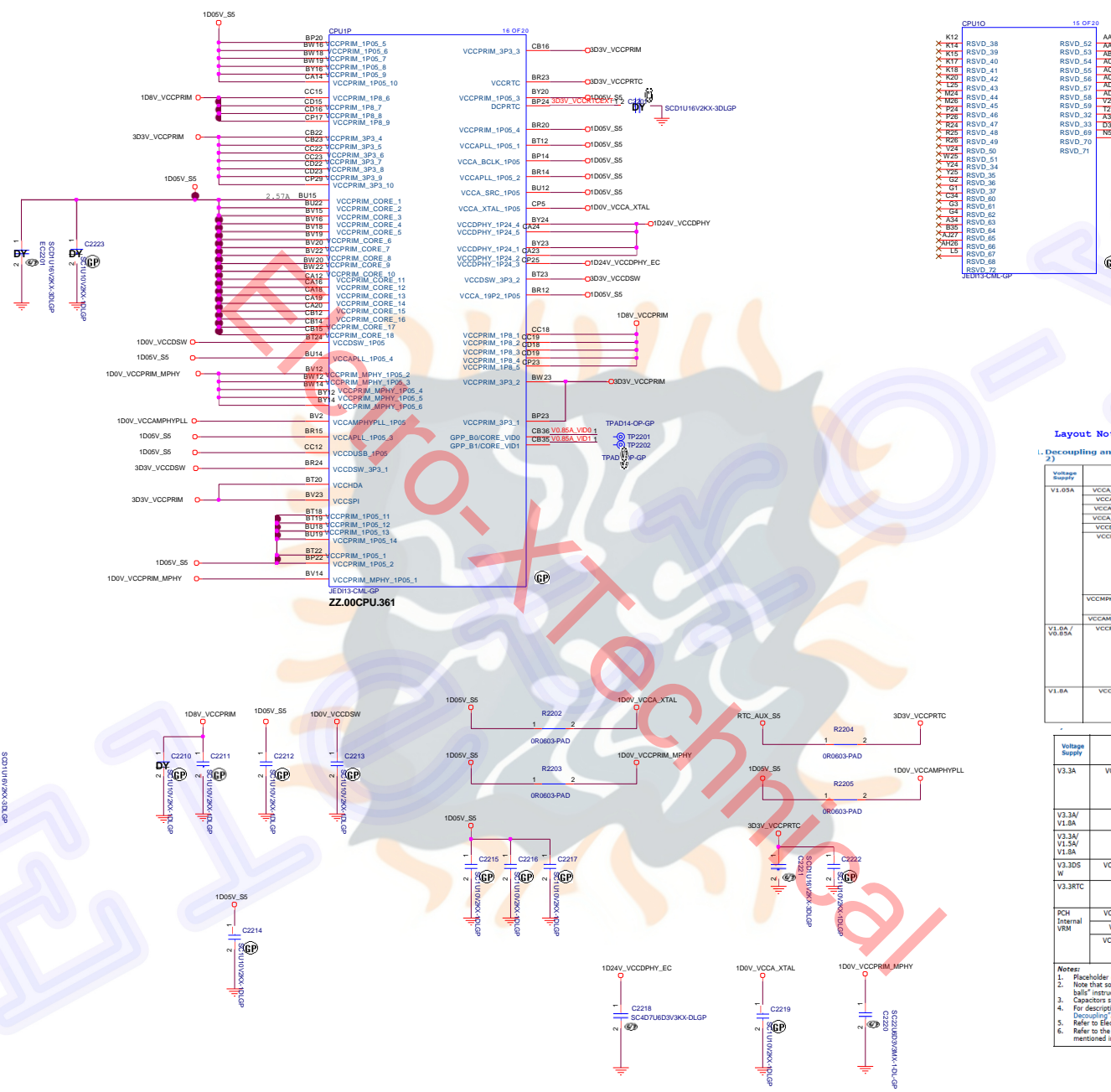
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14 UMA non interleaved	0	0
15 UMA non interleaved	0	1
14 DIS interleaved	1	0
15 DIS interleaved	1	1



(PDG#543016) Ensure that all I2C interface on-board terminations are pulled up to the same voltage rail as the device/end point.



PROJECT_ID[3:2]	Project Type	11	Inspiron
		10	Vostro
		01	Latitude (Reserved)
		00	N/A
PROJECT_ID[1:0]	Project Series	11	3000 Series
		10	5000 Series
		01	7000 Series
		00	N/A



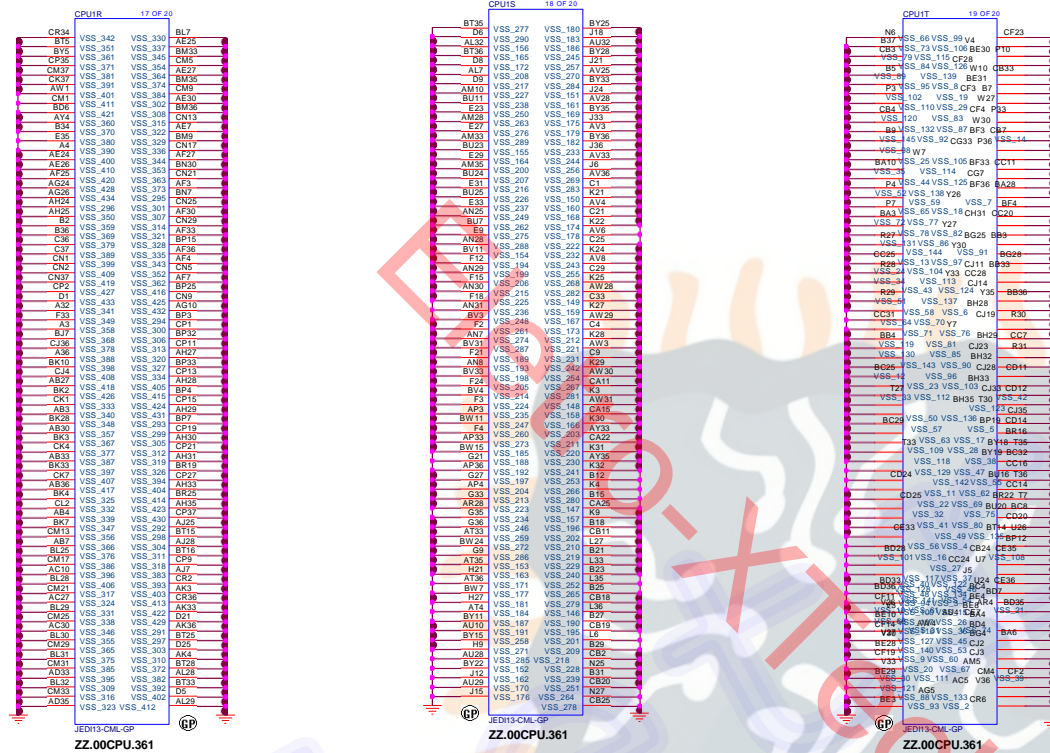
### Layout Note:

#### 1. Decoupling and Power Connection Requirements for WHL U PCH (Sheet 1 of 2)

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (1st priority / 2nd priority)	Place capacitor(s) near ball(s)
V1.05A	VCCA_1P05_1P05	BR12	-	-	-	-	-
	VCCA_OC_1P05	BP14	-	-	-	-	-
	VCCA_SRC_1P05	BU12	-	-	-	-	-
	VCCA_XTAL_1P05	CP5	1uF	0402	1	E	CP5
	VCCDSW_1P05	CC12	-	-	-	-	-
	VCCPRIM_1P05	BT12, BR14, BP14, BU12, BV12, BW12, BY12, CA12, CB12, CC12, CD12, CE12, CF12, CG12, CH12, CI12, CJ12, CK12, CL12, CM12, CN12, CO12, CP12, CQ12, CR12, CS12, CT12, CU12, CV12, CW12, CX12, CY12, CZ12	1uF	0402	1	E	BP20
	VCCMPHYVSTAGN_1P05	BU12, BV12, BW12, BY12, CA12, CB12, CC12, CD12, CE12, CF12, CG12, CH12, CI12, CJ12, CK12, CL12, CM12, CN12, CO12, CP12, CQ12, CR12, CS12, CT12, CU12, CV12, CW12, CX12, CY12, CZ12	22uF	0603	1	E	BU12
	VCCAMPHYVLL_1P05	BV12	1uF	0402	1	E	BV12
V1.05A V0.85A	VCCPRIM_CORE	BU12, BV12, BW12, BY12, CA12, CB12, CC12, CD12, CE12, CF12, CG12, CH12, CI12, CJ12, CK12, CL12, CM12, CN12, CO12, CP12, CQ12, CR12, CS12, CT12, CU12, CV12, CW12, CX12, CY12, CZ12	1uF	0402	1	E	BU12, Note 1
V1.05A	VCCPRIM_1P05	BU12, BV12, BW12, BY12, CA12, CB12, CC12, CD12, CE12, CF12, CG12, CH12, CI12, CJ12, CK12, CL12, CM12, CN12, CO12, CP12, CQ12, CR12, CS12, CT12, CU12, CV12, CW12, CX12, CY12, CZ12	1uF	0402	1	E	CP17

Voltage Supply	Area	PCH Pins sharing power rail	Value	Size	Quantity	Placement type (1st priority / 2nd priority)	Place capacitor(s) near ball(s)
V3.3A	VCCPRIM_3P3	CB22, CB23, CC22, CC23, CD22, CD23, CP22, CP23, BP23, CB16	0.1uF	0402	1	E	CP23, Note 1
			1uF	0402	1	E	CP23, Note 1
V3.3A/V1.5A	VCCSPI	BV23	-	-	-	-	-
V3.3A/V1.5A/V1.5A	VCCCHDA	BT20	-	-	-	-	-
V3.305W	VCCDSW_GRP0	BR24, BT23	1uF	0402	1	E	BR24, Note 1
V3.3RTC	VCCRTC	BR23	1uF	0402	1	E	BR23
			0.1uF	0402	1	E	-
PCH Internal VMM	VCCDSW_1P05	BT24	1uF	0402	1	E	BT24
	VCCRTCEXT	BP24	1uF	0201	1	E	BP24, Note 1
	VCCDPHY_1P24	BY23, CA23, CP25, BV24, CA24	4.7uF	0402	1	E	CP25

- Notes:
1. Placeholder only. Does not need to be stuffed.
  2. Note that some decoupling capacitors are shared between more than 1 rail. Follow the "Place capacitors near ball(s)" instructions above to ensure this sharing is optimized.
  3. Capacitors should be placed less than 100 mils (2.54 mm) from the edge of package.
  4. For description of (1st priority, and (2nd priority) capacitor placement, refer to "Loop Inductance Reduction Decoupling".
  5. Refer to Electromagnetic Interference chapter for recommended placement.
  6. Refer to the vendor requirements for bulk decoupling which will be in addition to the recommendation mentioned in the table above.



Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

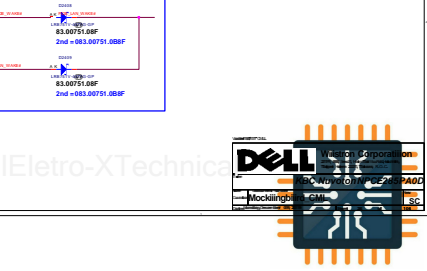
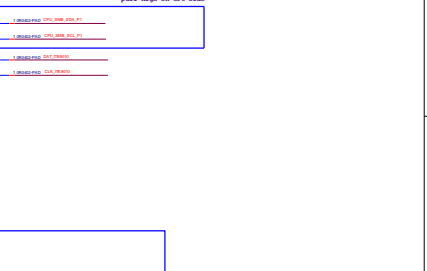
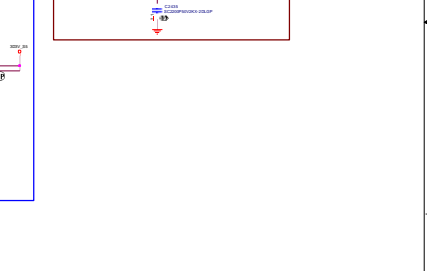
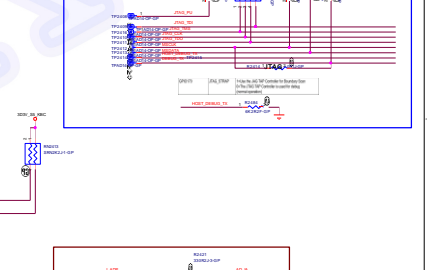
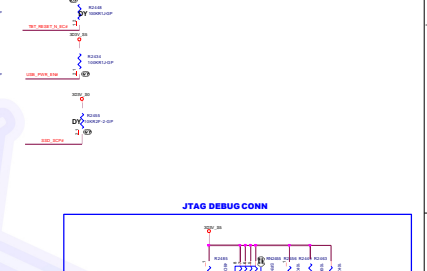
&lt;Core Design&gt;



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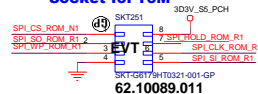




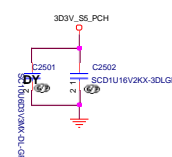
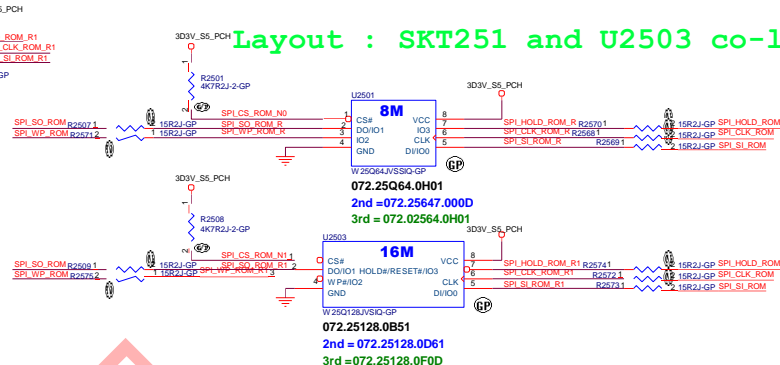
# SSID = SPI Flash

18,24 SPI\_CS\_ROM\_N1 >>>  
 18,24 SPI\_CS\_ROM\_N0 >>>  
 18,24 SPI\_SO\_ROM <<<  
 18,24 SPI\_CLK\_ROM >>>  
 15,18,24 SPI\_SI\_ROM >>>  
 15,18,24 SPI\_HOLD\_ROM <<<  
 15,18,24 SPI\_WP\_ROM <<<

## Socket for 16M

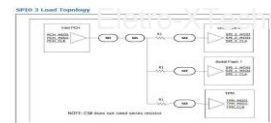


## Layout : SKT251 and U2503 co-lay



## Dual SPI Devices + TPM Topology Guidelines

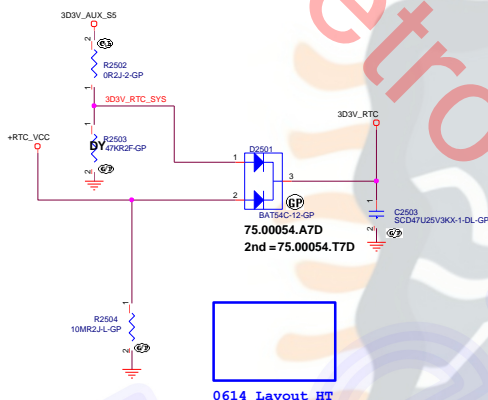
The CFL PCH supports TPM through SPI0 bus. The topology below was a full configuration which consist of 2 SPI0 Flash and 1 TPM device. The system can be configured with 1 SPI0 Flash and 1 TPM device.



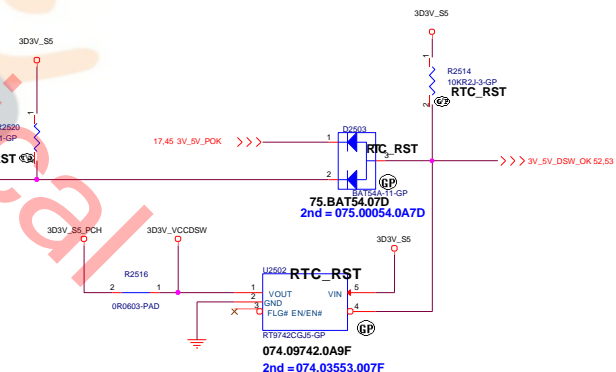
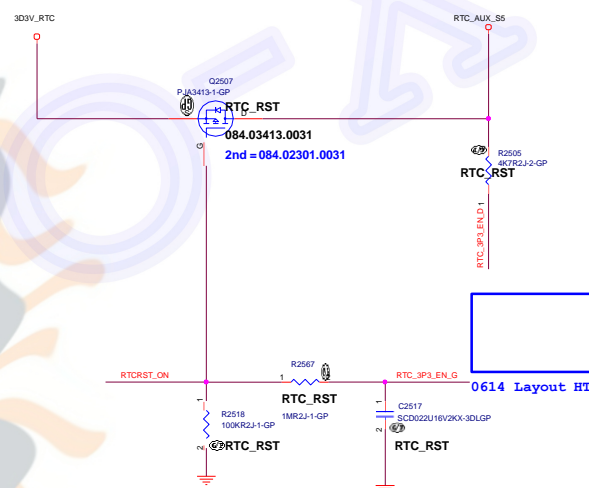
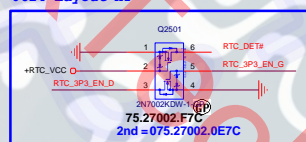
Segment	Trace Type	Reference	Via Count	Max Length, mm	Max Length, mils
Segment	Total	Segment	Total	Segment	Total
Notes:					
1. R1 Resistor should be 18 ohm for 1.8V and 33 ohm for 3.3V. SPI0_VCC and SPI0_VDD connection to be pulled up with 1k ohm on R2 position.					
2. R number of 1k ohm can be allowed.					
3. Reference plane should be continuous Ground Plane only allowed.					
4. This topology relates to SPI0_F0, F1, F2, F3, F4, SPI0_P0CS, SPI0_P0CS0 and SPI0_CLK.					
5. Design guideline support up to 50MHz.					

# SSID = RTC

15,20 RTC\_DET# <<<  
 24 VCCDSW\_EN >>>  
 24 RTCRST\_ON >>>



## 0614 Layout HT



Eletro-XTechnical

Eletro-X

Eletro-XTechnical

«Come Design»

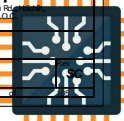
**DELL** Wistron Corporation

2/F, 8/F, Sec. L, Hsin-Tai W. Rd., Taipei 105, Taiwan, R.O.C.

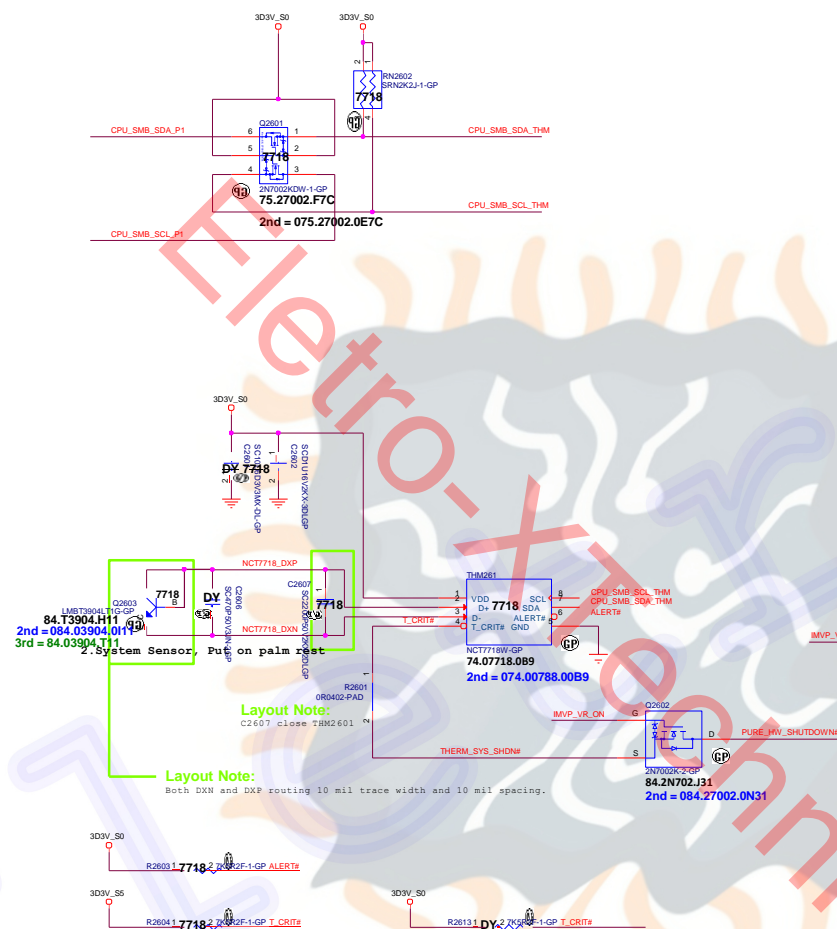
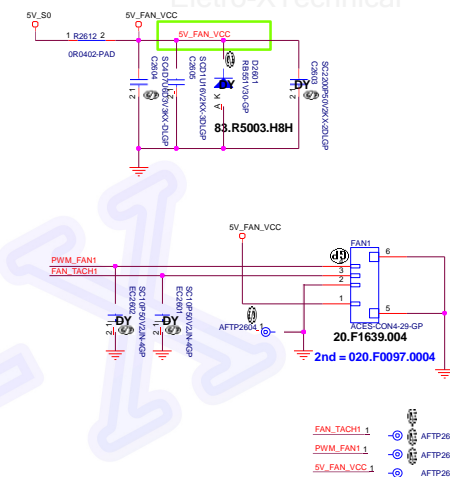
**Flash**

Mockingbird\_CML

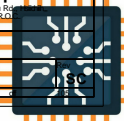
Monday, December 10, 2018



**Layout Note:**  
Signal Routing Guideline:  
Trace width = 15mil



TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



SSID = Audio

19 HDA\_SDIN0\_CPU <<< \_\_\_\_\_

19 HDA\_SDOUT\_CODEEC >>> \_\_\_\_\_

19 HDA\_SYNC\_CODEEC >>> \_\_\_\_\_

19 HDA\_BITCLK\_CODEEC >>> \_\_\_\_\_

29 AUD\_SPK\_R+ <<< \_\_\_\_\_

29 AUD\_SPK\_R- <<< \_\_\_\_\_

29 AUD\_SPK\_L+ <<< \_\_\_\_\_

29 AUD\_SPK\_L- <<< \_\_\_\_\_

```

24 NB_MuteIn    >>> _____
15,19 SPKR      >>> _____
24 BEEP         >>> _____
66 AUD_SENSE    >>> _____
29 LINE1_VREF0  <<< _____
29 MIC2_VREF0   <<< _____
9 AUD_HP1_JACK_L <<< _____
AUD_HP1_JACK_R  <<< _____
29 LINE1_L      >>> _____
29 LINE1_R      >>> _____

```

```

29,66 AUD_SLEEVE <<<_____
29,66 AUD_RING  <<<_____

55 DMIC_SCL_CODEC <<<_____
55 DMIC_SDA_CODEC <<<_____

17,40,55 PM_SLP_S3# >>>_____

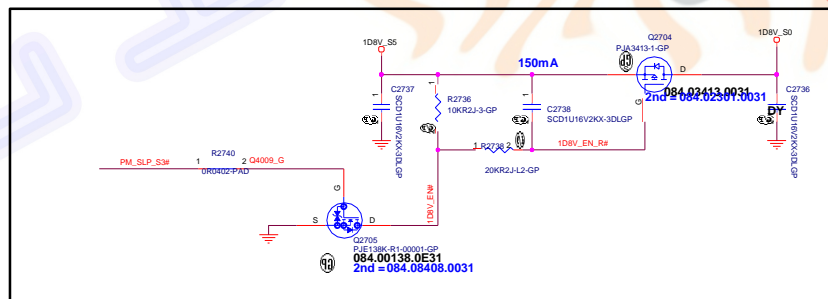
```

**Azalia I/F EMI**  
HDA\_SDOUT\_CODEC  
HDA\_BITCLK\_CODEC

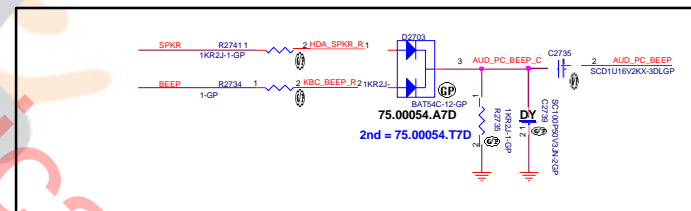
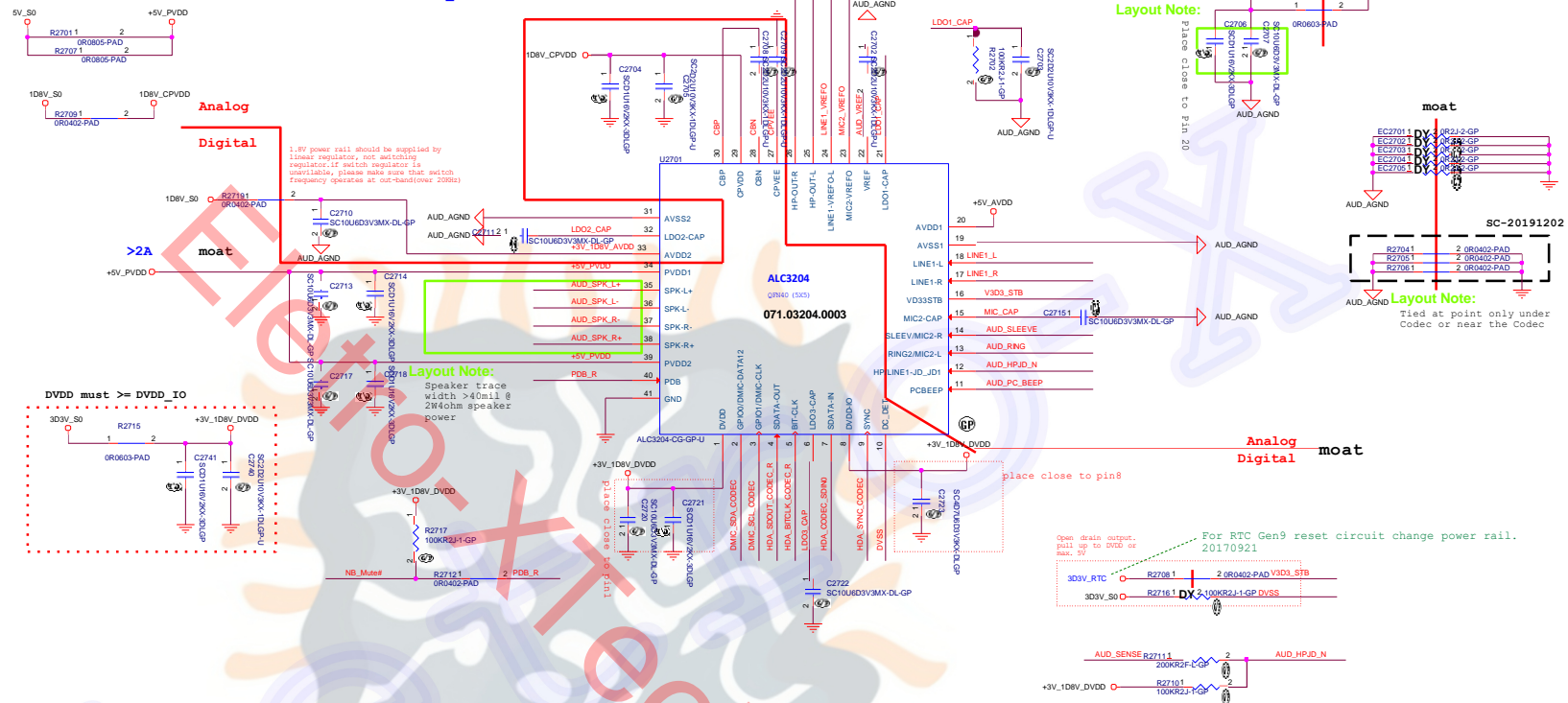
HDA\_SDIN0\_CPU R2724 1 2 2R2J-2-GP HDA\_CODECS\_SDIN0

HDA\_SDOUT\_CODECS R2722 1 2 0R0402-PAD HDA\_SDOUT\_CODECS

HDA\_BITCLK\_CODECS R2723 1 2 33R2J-2-GP HDA\_BITCLK\_CODECS



## Audio Codec Chip ALC3204



«Come Design»



**Wistron Corporation**  
21F., 88, Sec. 1, Hsin Tai Wu Rd., Taipei 100, Taiwan

Taipei Hsien 221, Taiwan, R.O.C.

<b>Audio Codec ALC3234</b>	
Size	Document# Number

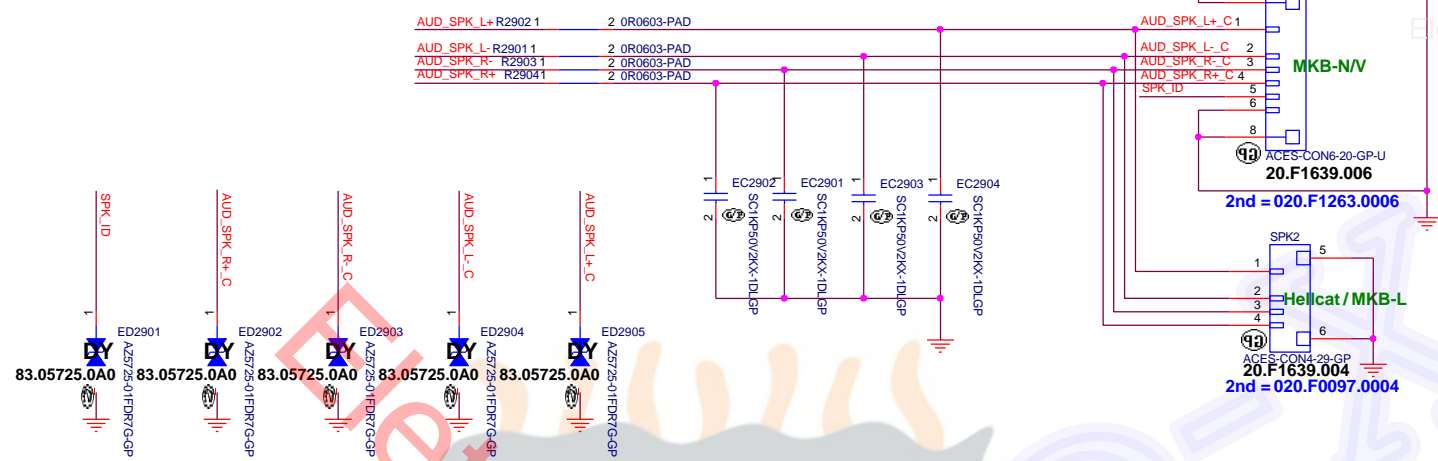
A2	<i>Mockingbird_CML</i>
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Date: Monday, December 09, 2019 Sheet: 27

SSID = Audio

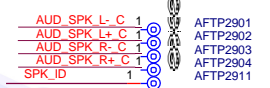
Layout Note:  
Speaker trace width >40mil @ 2W4ohm speaker power

Speaker

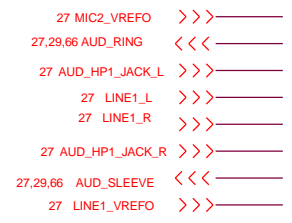


CONN Pin	Net name
Pin1	SPK_L+
Pin2	SPK_L-
Pin3	SPK_R-
Pin4	SPK_R+
Pin5	SPK_DET#
Pin6	GND

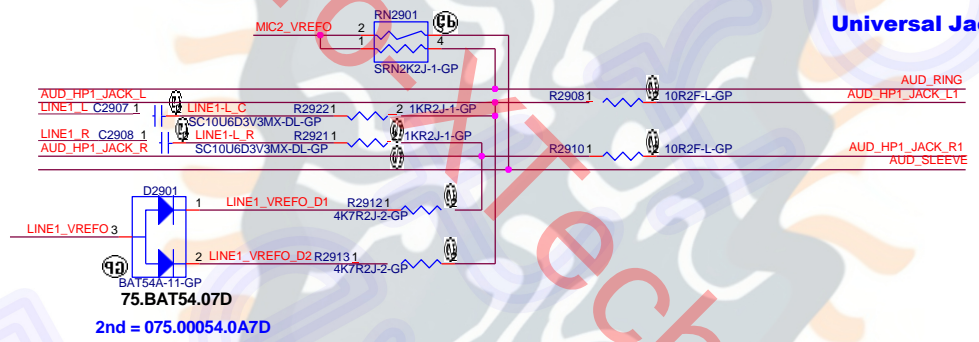
SPK\_ID 1: FG  
0: Veci



From Codec



Universal Jack (Moved to I/O Board)



To IO Board



<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec. 1, HsinTaiWu Rd., Hsichih,  
Taipei-Hsien 221, Taiwan, R.O.C.

Audio IO

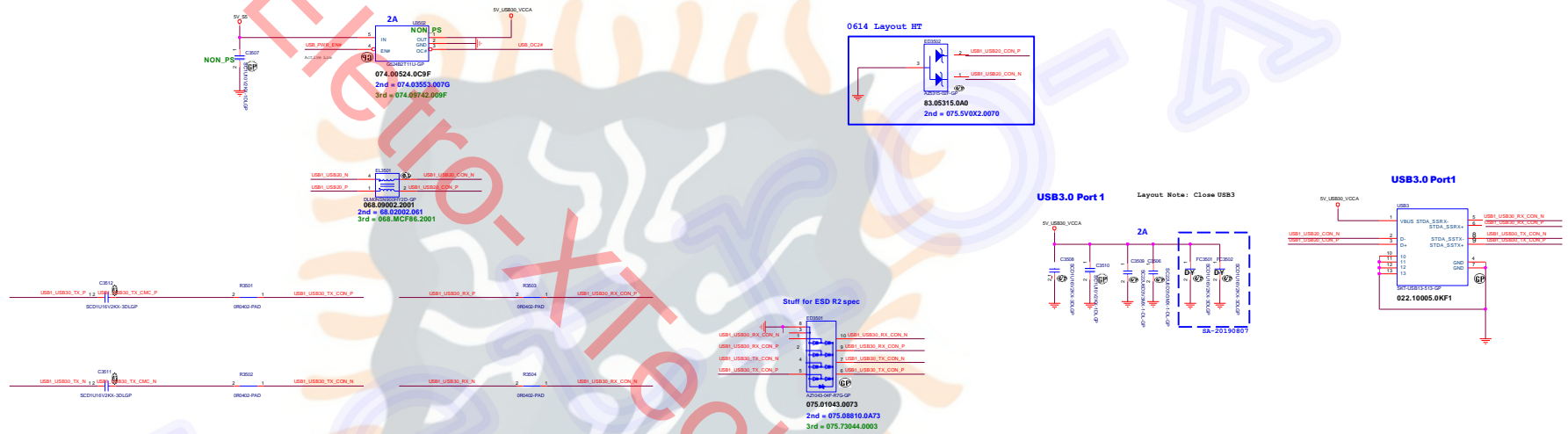
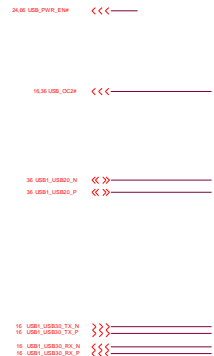
Mockingbird CML

Date: Monday, December 09, 2019

Sheet 29 of 30



SSID = USB3.0 Port1

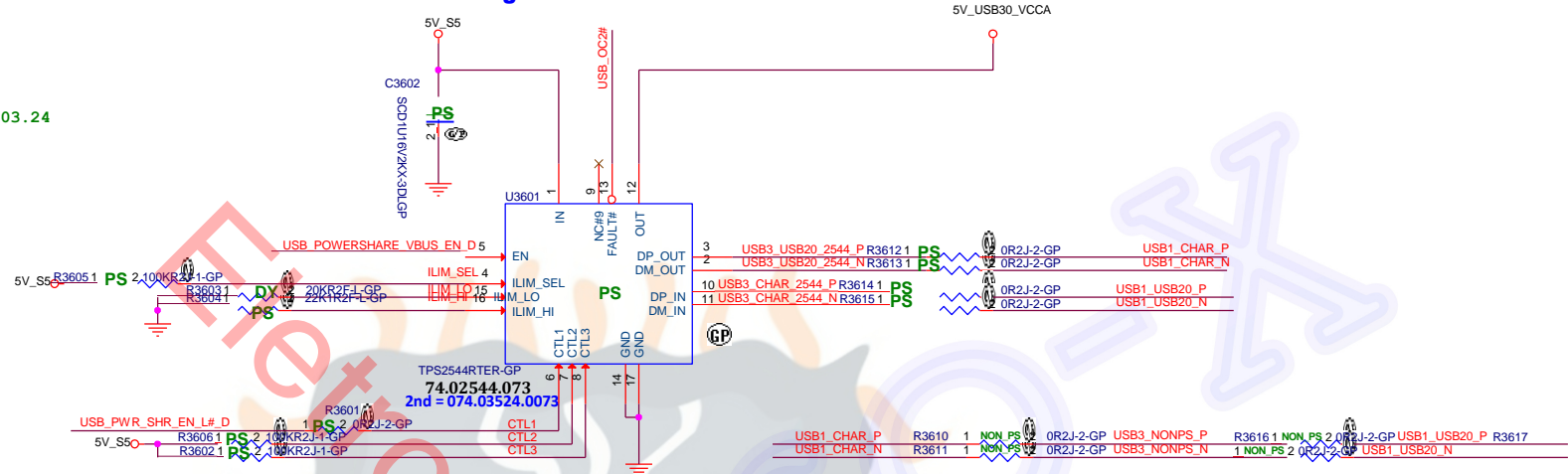


Main Func = USB3.0 Port2



2018.03.24

### USB Charger Port1



Device Control Pins				
	CTL1 (EC control)		CTL3	
<b>CDP</b>	1	1	1	1
<b>DCP Auto</b>	0	1	1	X

The following equation programs the typical current limit:

$$I_{OS\_DP} (mA) = \frac{50,500}{(R_{ILIM\_XX} (k\Omega) + 0.1)}$$

R<sub>ILIM\\_XX</sub> corresponds to either R<sub>ILIM\_HI</sub> or R<sub>ILIM\_LO</sub> as appropriate.

BOLT 15 32bit0822

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, Taipei-Hsien221, Taiwan, R.O.C.	
Title: <b>USB Charger</b>			
Size: Custom	Document Number: <b>Mockingbird_CML</b>		Rev: <b>SC</b>
Date: Monday, December 09, 2019	Sheet 36	of	105



5V\_S0 & 3D3V\_S0

11.27.55 PM\_SLP\_S0M >>>

HW\_SHUTDOWN

46 3V\_SV\_EN <<<

26 PURE\_HV\_SHUTDOWNM >>>

24 ALDSON >>>

POWER GOOD

51 100V\_VTT\_PWRGD >>>

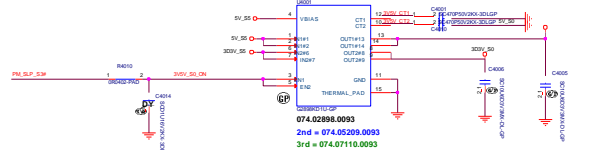
VCCIO & VCCSTG

21 GPRC\_HIS\_BOOTMFC <<<

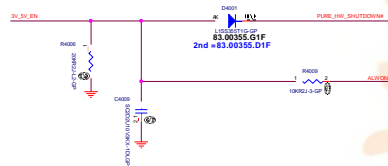
17.24.44.65 VCCST\_PWRGD <<<

17.24.02.65.61 PLS\_RSTM >>>

## ROSA Run Power



## ROSA Run Power



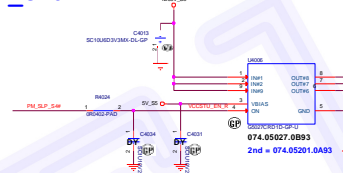
## MANAGEMENT RAIL POWER GENERATION

VCCST, VCCSTG, and VCCSTL can remain powered during S4 and S5 power states for board VS optimization.

VCCST\_CPU

17.21.66 PM\_SLP\_S0M >>>

VCCST\_CPU

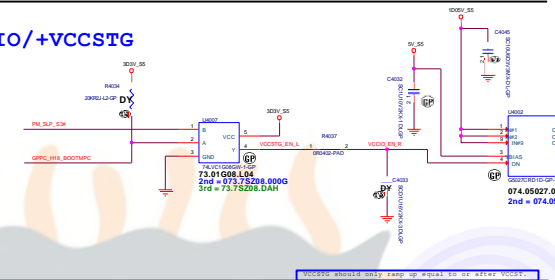


5V\_S0  
5V\_S0 Consumption  
Peak Current: 5A  
3D3V\_S0  
3D3V\_S0 Consumption  
Peak Current: 2.5A

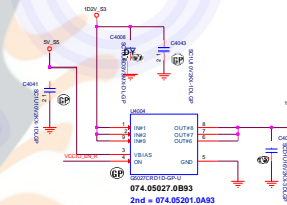
## Power Good



## +VCCIO/+VCCSTG

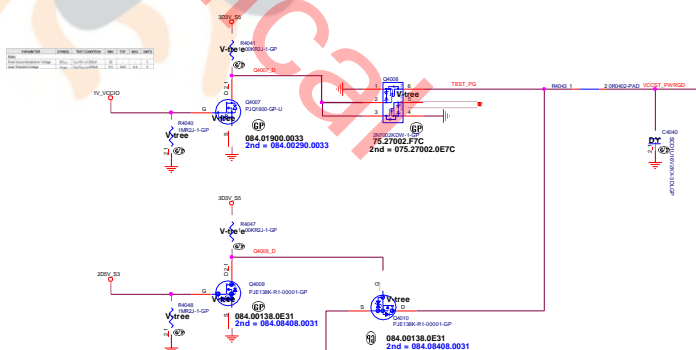


## 1D2V\_VCCSFR\_OC



VCCST\_CPU

## V-tree\_VCCIO



Eletro-XTechnical

Eletro-XTechnical

Eletro-XTechnicalEletro-XTe

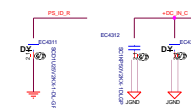
SSID = ADT Input

24.4K AC\_DS &gt;&gt;&gt;

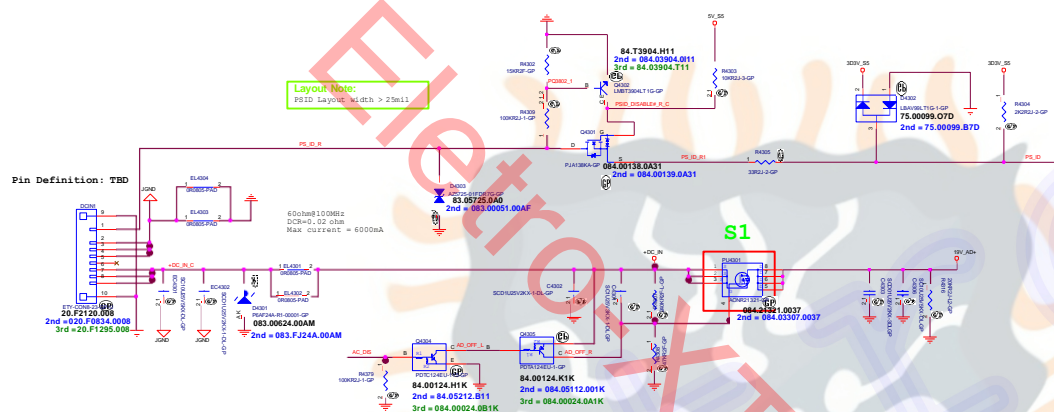
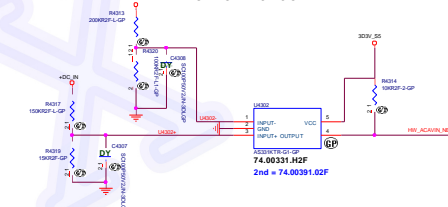
24.4K PS\_ID &lt;&lt;&lt;

24.4K WEL\_ACAV15B &lt;&lt;&lt;

88 +DC\_RN\_C &lt;&lt;&lt;

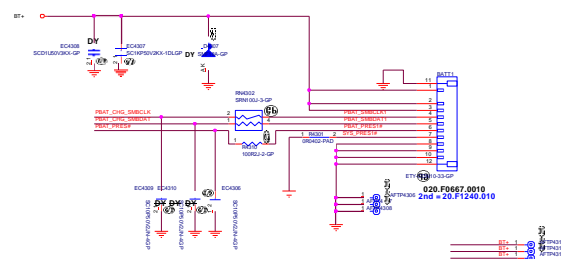


### Barrel Adapter Plug-in Detect Follow Bandon



SSID = M-BAT Input

### Batt Connector



24.4K PRAT\_CHG\_SMBCLK &lt;&lt;&lt;

24.4K PRAT\_CHG\_SMBDAT &lt;&lt;&lt;

24.4K PRAT\_PRESH &lt;&lt;&lt;

Eletro-XTechnical

Eletro-XTechnicalEletro-XTechnical



OFFPAGE

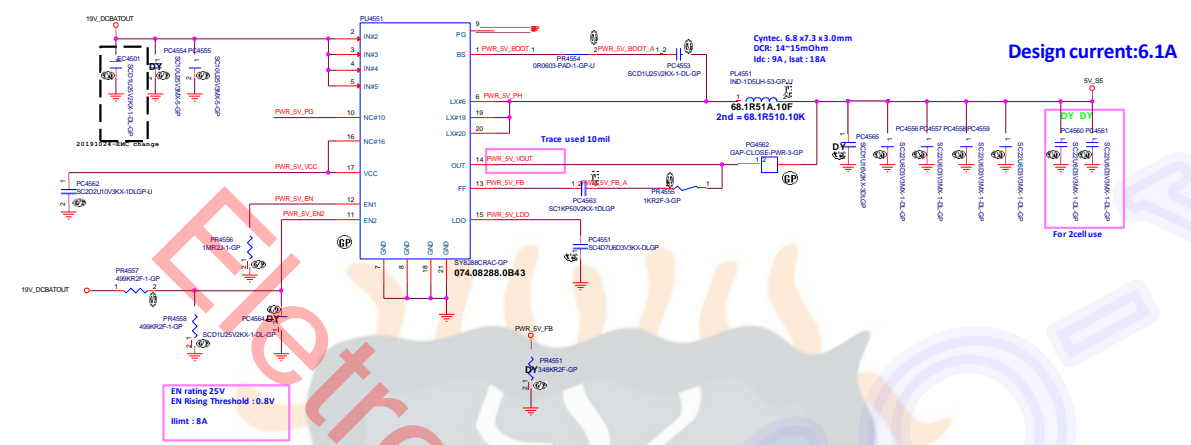
SSID = PWR.Plane.Regulator\_5V

OFFPAGE-Signal

OFFPAGE-GAP



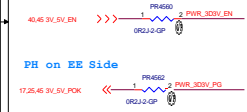
# SY8288C For 5V



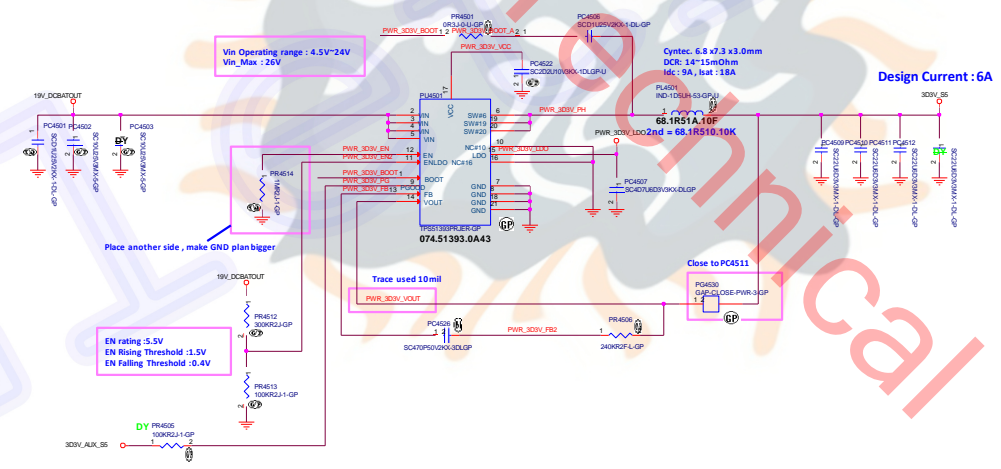
SSID = PWR.Plane.Regulator\_3D3V

OFFPAGE-Signal

OFFPAGE-GAP



# TPS51393 For 3D3V



PH on CPU side

**PH on CPU side**

3,24,44 PREDICT#_CPU	<<<
7 SVD_ALERT#_CPU	<<<
7 SVD_CLK_CPU	>>>
7 SVD_DATA_CPU	>>>
17,44 PWR_RMP_PWRGD	>>>
17,34,44-VCT#_PWRGD	>>>

For VCCGT Sense

8 VDDGT\_SENSE >>—————

8 VDDGT\_SENSE >>—————

**For Vcore Sense**

7 VDDCORE\_SENSE >>—

7 VSSCORE\_SENSE >>—

For Vccsa Sense

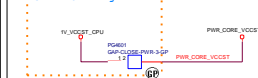
8 VSSSA\_SENSE      >> \_\_\_\_\_

8 VCSA\_SENSE      >> \_\_\_\_\_

```

.....
: EE side Link
: SVID Pull High V

```



```

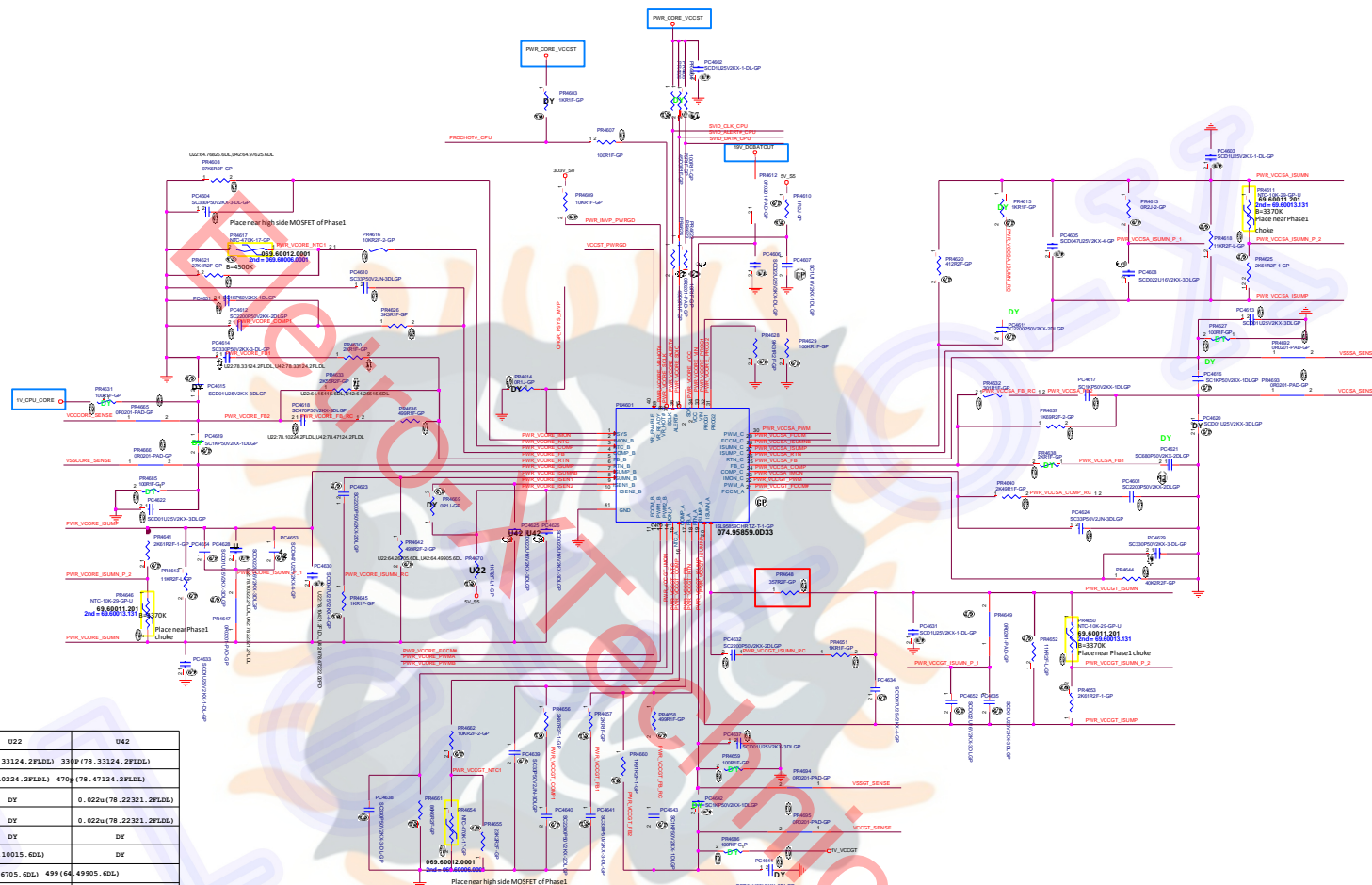
47 PWR_VCORE_PVMB    >>>
47 PWR_VCORE_ISUN     >>>
47 PWR_VCORE_ISUMP    >>>
47 PWR_VCORE_FCCM#   >>>
47 PWR_VCORE_PVMA     >>>
48 PWR_VCCGT_PWM      >>>
48 PWR_VCCGT_FCCM#    >>>
48 PWR_VCCGT_ISUN     >>>
48 PWR_VCCGT_ISUMP    >>>
50 PWR_VCCSA_ISUMP    >>>
50 PWR_VCCSA_ISUN     >>>
50 PWR_VCCSA_PWM      >>>
50 PWR_VCCSA_FCCM#    >>>

```

```
47 PWR_VCORE_ISEN1 >>>_____
47 PWR_VCORE_ISEN2 >>>_____
```

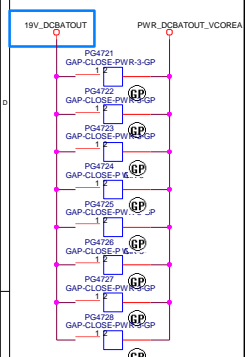
4. CHGB PSYS MVP >>>

	U22	U42
PC4614	330P (78.33124, 2FL10L)	330P (78.33124, 2FL10L)
PC4618	18P (78.40234, 2FL10L)	770P (78.47124, 2FL10L)
PC4625	DY	0.022u (78.22321, 2FL10L)
PC4626	DY	0.022u (78.22321, 2FL10L)
PR4669	DY	DY
PR4670	1R (64.10015, 6DL)	DY
PR4672	2.97 (64.28703, 6DL)	489P (64.49905, 6DL)
PC4630	0.1uP (78.40451, 2FL10L)	47uP (078.47322, 02P)
PC4628	0.01uP (78.10322, 2FL10L)	22uP (78.02321, 2FL10L)
PC4654	DY	0.012uP (78.10322, 2FL10L)
PC4653	DY	47uP (078.47322, 02P)
PR4633	1.54K (64.14515, 6DL)	2.55K (64.25515, 6DL)
PR4608	76.8K (64.76825, 6DL)	97K (64.97625, 6DL)

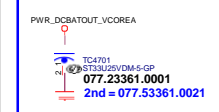


SSID = CPU CORE

OFFPAGE



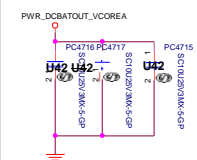
For acoustic noise



```

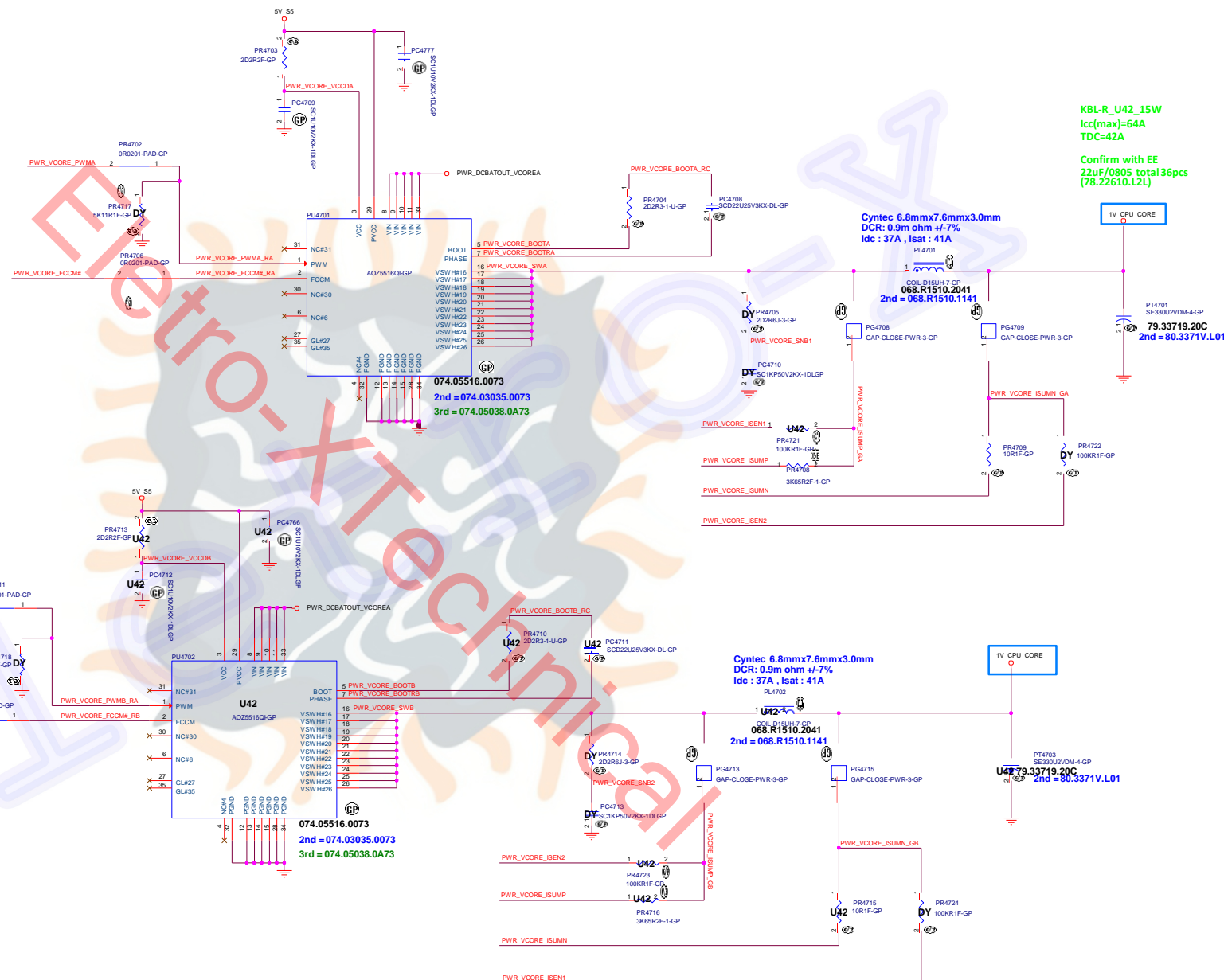
46 PWR_VCORE_PWMA
46,47 PWR_VCORE_FCCM#
46,47 PWR_VCORE_ISEN1
46,47 PWR_VCORE_ISUMP
46,47 PWR_VCORE_ISUMN
46,47 PWR_VCORE_ISEN2

```



46 PWR\_VCORE\_PWMB  
46,47 PWR\_VCORE\_FCCM#  
46,47 PWR\_VCORE\_ISEN2  
46,47 PWR\_VCORE\_ISUMP  
46,47 PWR\_VCORE\_ISUMN  
46,47 PWR\_VCORE\_ISEN1

# AOZ5516Q For VCORE



KBL-R\_U42\_15W  
Icc(max)=64A  
TDC=42A

Confirm with EE  
22uF/0805 total 36pcs  
(78.22610.L2L)

PT4701  
SE330U2VDM-4-GP  
79.33719.20C  
2nd = 80.3371V.L01

Eletro-XTechnical

# Eletro-X

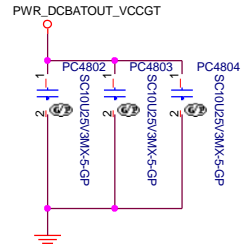
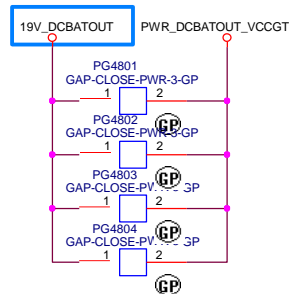


SSID = CPU\_CORE

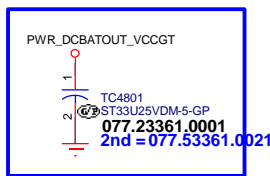
Offpage-Signal

# AOZ5516Q For VCCGT

Eleto-X Technical



For acoustic noise



46 PWR\_VCCGT\_PWM  
46 PWR\_VCCGT\_FCCM#  
46 PWR\_VCCGT\_ISUMN  
46 PWR\_VCCGT\_ISUMN

PR4802  
0R0201-PAD-GP

PWR\_VCCGT\_PW2M

1

PR4812  
5K11R1F-GP

PR4806  
0R0201-PAD-GP

PWR\_VCCGT\_FCCM#

2

1

PWR\_VCCGT\_PWM\_R

PWR\_VCCGT\_FCCM#\_R

1

2

1

2

1

2

1

2

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1

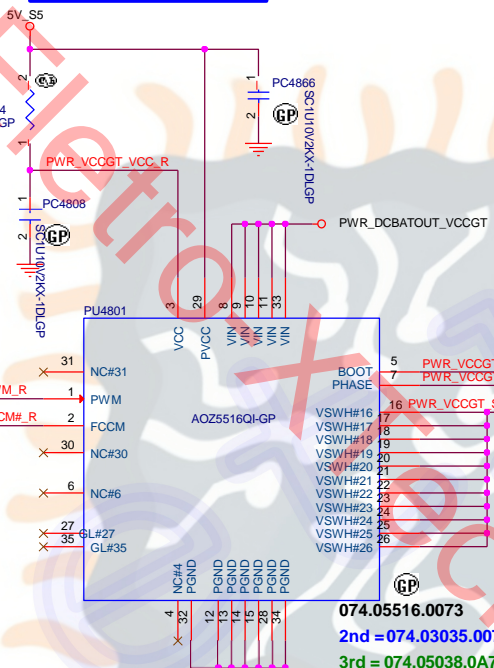
2

1

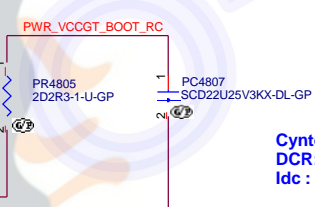
2

1

2



074.05516.0073  
2nd = 074.03035.0073  
3rd = 074.05038.0A73



Cyntec 6.8mmx7.6mmx3.0mm  
DCR: 0.9m ohm +/-7%  
Isc : 37A , Isat : 41A

KBL\_U22\_15W  
Icc(max)=31A  
TDC=21A

Confirm with EE  
22uF/0805 total 33pcs  
(78.22610.L2L)

PL4801  
068.R1510.2041  
2nd = 068.R1510.1141

1V\_VCCGT  
PANASONIC  
ESR: 9mohm  
PT4801  
SE330U2VDM-4-GP  
79.33719.20C  
2nd = 80.3371V.L01

Wistron Corporation  
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin,  
Taipei-Hsien 221, Taiwan, R.O.C.

POWER (5036 CPU\_VCORE(3))

Size: A3  
Document Number: Mockingbird\_CML

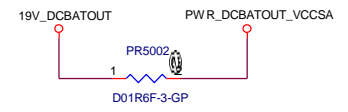
Date: Monday, December 09, 2019  
Sheet: 48 of 48



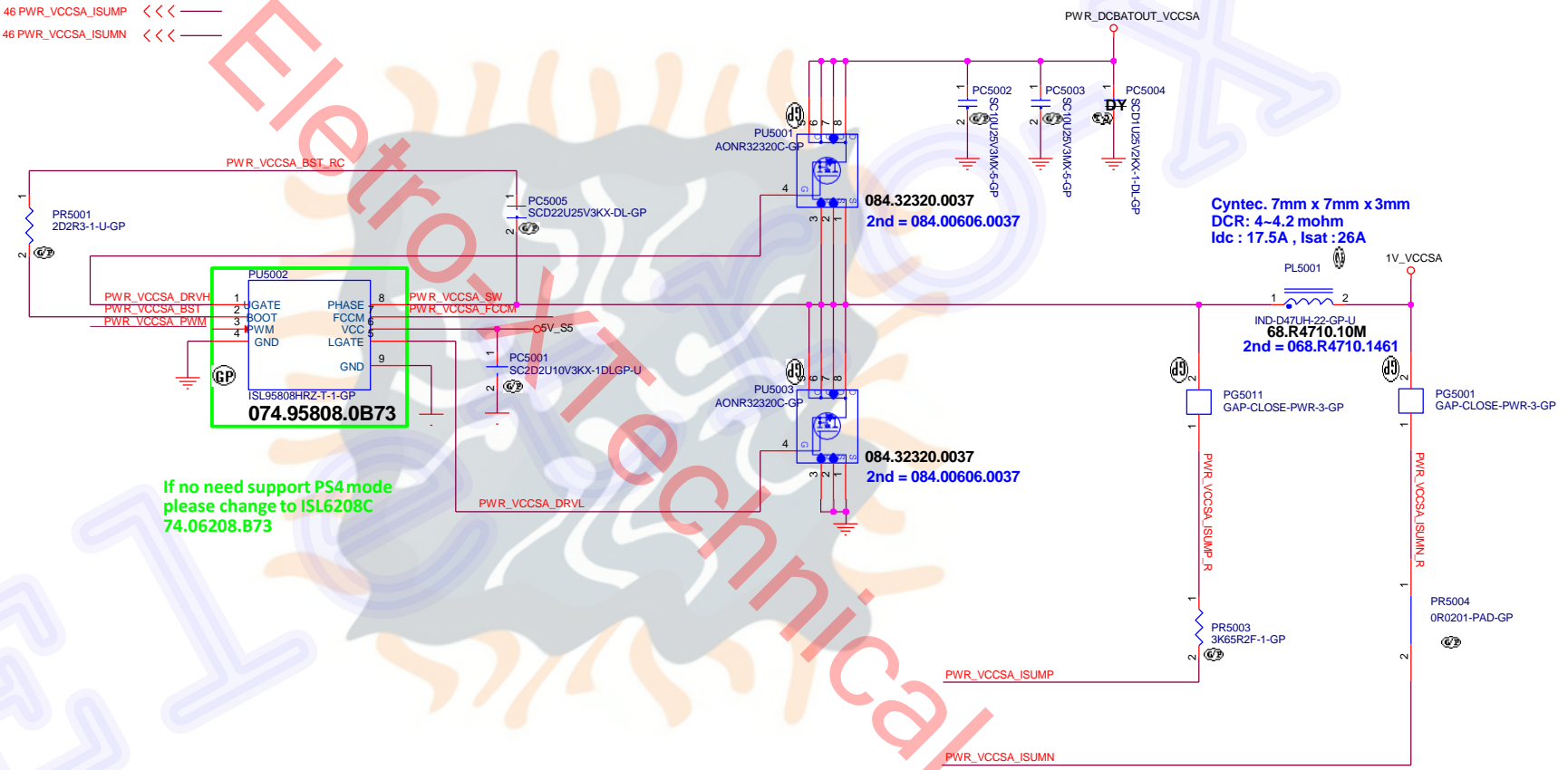
# ISL95808 For VCCSA


Eleto-X Technical

## OFFPAGE




- 46 PWR\_VCCSA\_PWM >>>
- 46 PWR\_VCCSA\_FCCM >>>
- 46 PWR\_VCCSA\_ISUMP <<<
- 46 PWR\_VCCSA\_ISUMN <<<

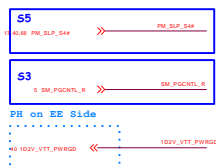


**Wistron Corporation**  
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Taipei-Hsien 221, Taiwan, R.O.C.

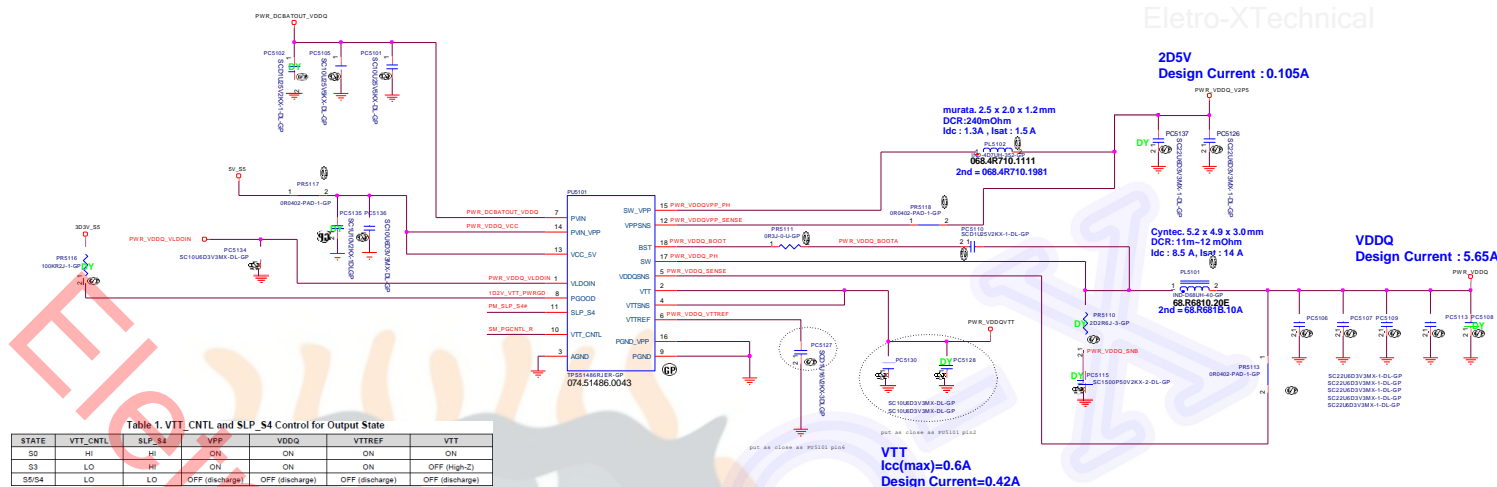
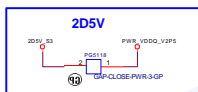
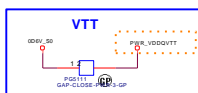
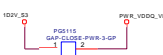
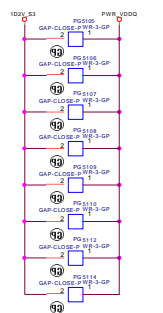
Title		POWER (ISL95808 VCCSA)	
Size	A3	Document Number	Mockingbird CML
Date:	Monday, December 09, 2019		Sheet 50 of



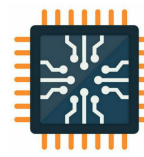
## OFFPAGE



## OFFPAGE GAP



STATE	VTT_CNTL	SLP_S4	VPP	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF (High-Z)
REISA	LO	LO	OFF (High-Z)	OFF (High-Z)	OFF (High-Z)	OFF (High-Z)



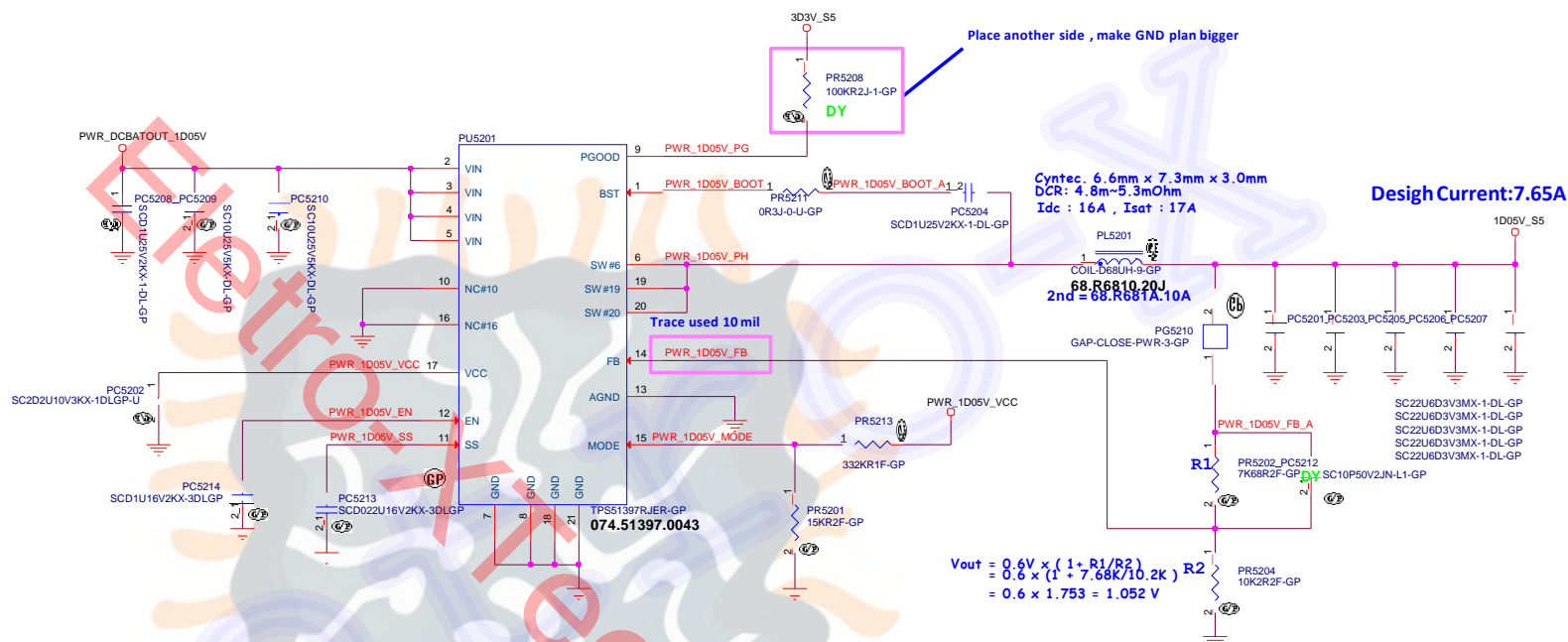
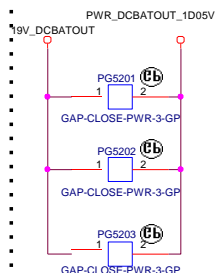
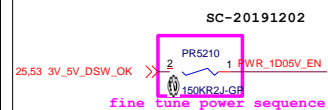
SSID = PWR.Plane.Regulator\_1D0V

OFFPAGE-Signal

OFFPAGE-GAP

# TPS51397 For 1D05V

EletoXTechnical



<Core Design>

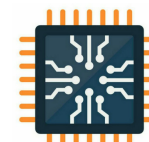
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichlin,  
Taipei Hsien 221, Taiwan, R.O.C.

POWER (TPS51397_1D05V)		
Size	Document Number	Rev
Custom	Mockingbird_CML	SC
Date:	Monday, December 09, 2019	Sheet 52 of 105

Eleto-XTechnical

Eleto-XTechnicalEleto-XTechnical

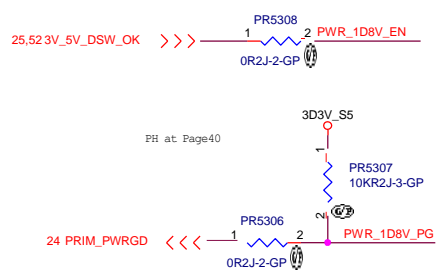
Eleto-X



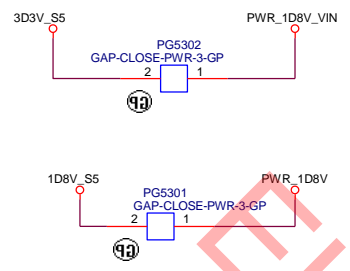


SSID = 1D8V

OFFPAGE

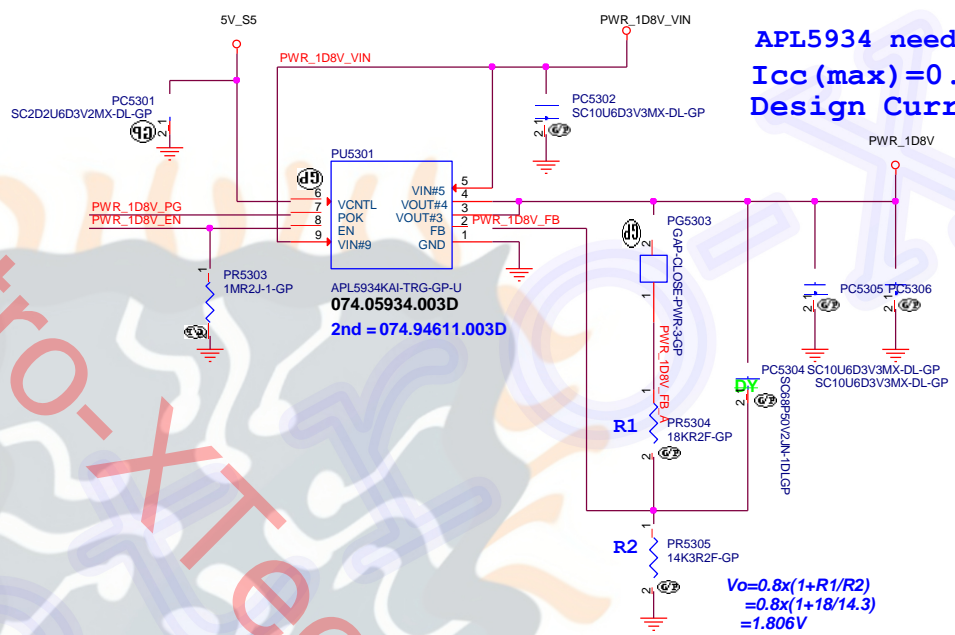


OFFPAGE\_GAP



APL5934 for 1D8V

Eletro-XTechnical



Eletro-XTechnical

Eletro-XTechnical

Eletro-X

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin, Taipei-Hsien 221, Taiwan, R.O.C.

**POWER (APL5934 1D8V)**

Size A3 Document Number Mockingbird CML 53

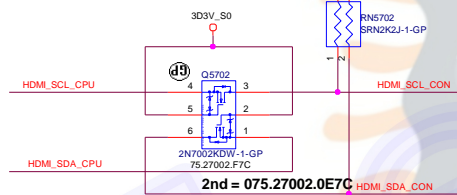
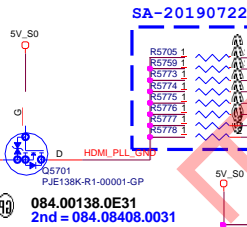
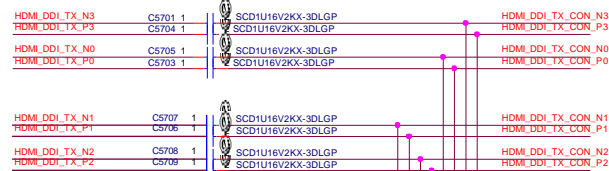
Date: Monday, December 09, 2019 Sheet 1 of 1



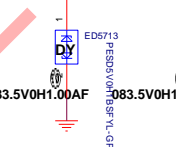
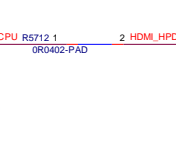
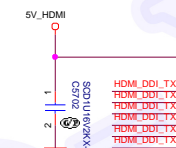
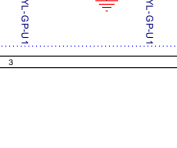
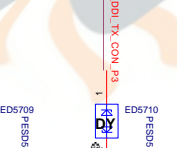
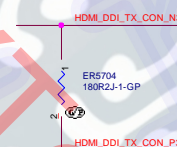
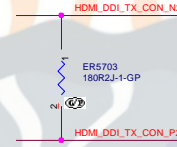
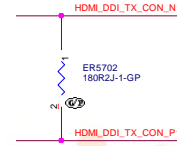
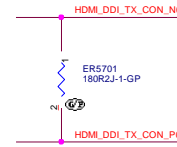
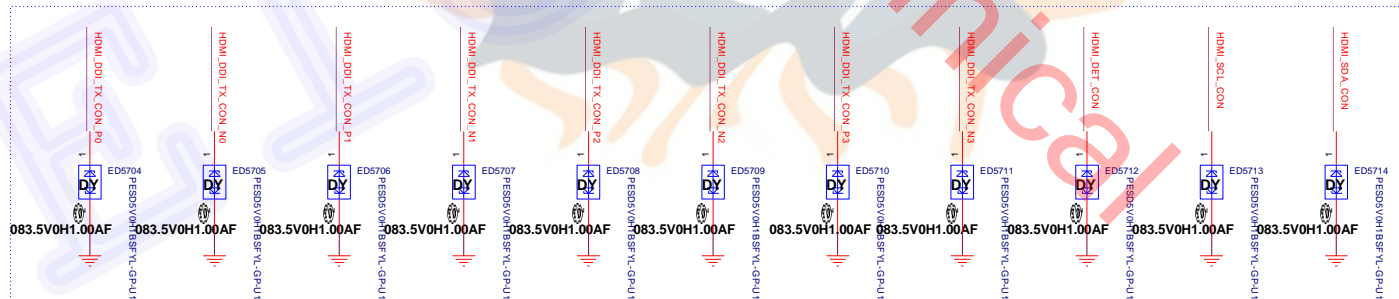
# SSID = HDMI Level Shifter/Connector

4 HDMI\_DDI\_TX\_N0 >>>  
4 HDMI\_DDI\_TX\_P0 >>>  
4 HDMI\_DDI\_TX\_N1 >>>  
4 HDMI\_DDI\_TX\_P1 >>>  
4 HDMI\_DDI\_TX\_N2 >>>  
4 HDMI\_DDI\_TX\_P2 >>>  
4 HDMI\_DDI\_TX\_N3 >>>  
4 HDMI\_DDI\_TX\_P3 >>>

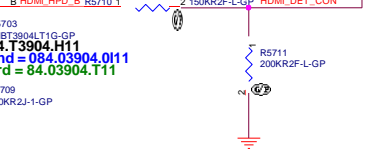
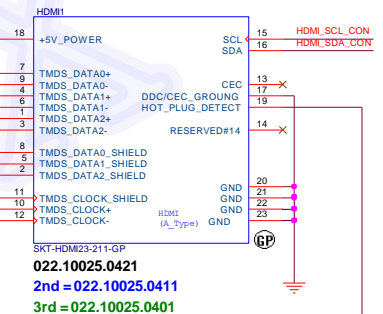
4 HDMI\_SCL\_CPU >>>  
4 HDMI\_SDA\_CPU >>>  
4 HDMI\_HPD\_CPU >>>



EMI Request:

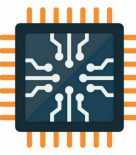


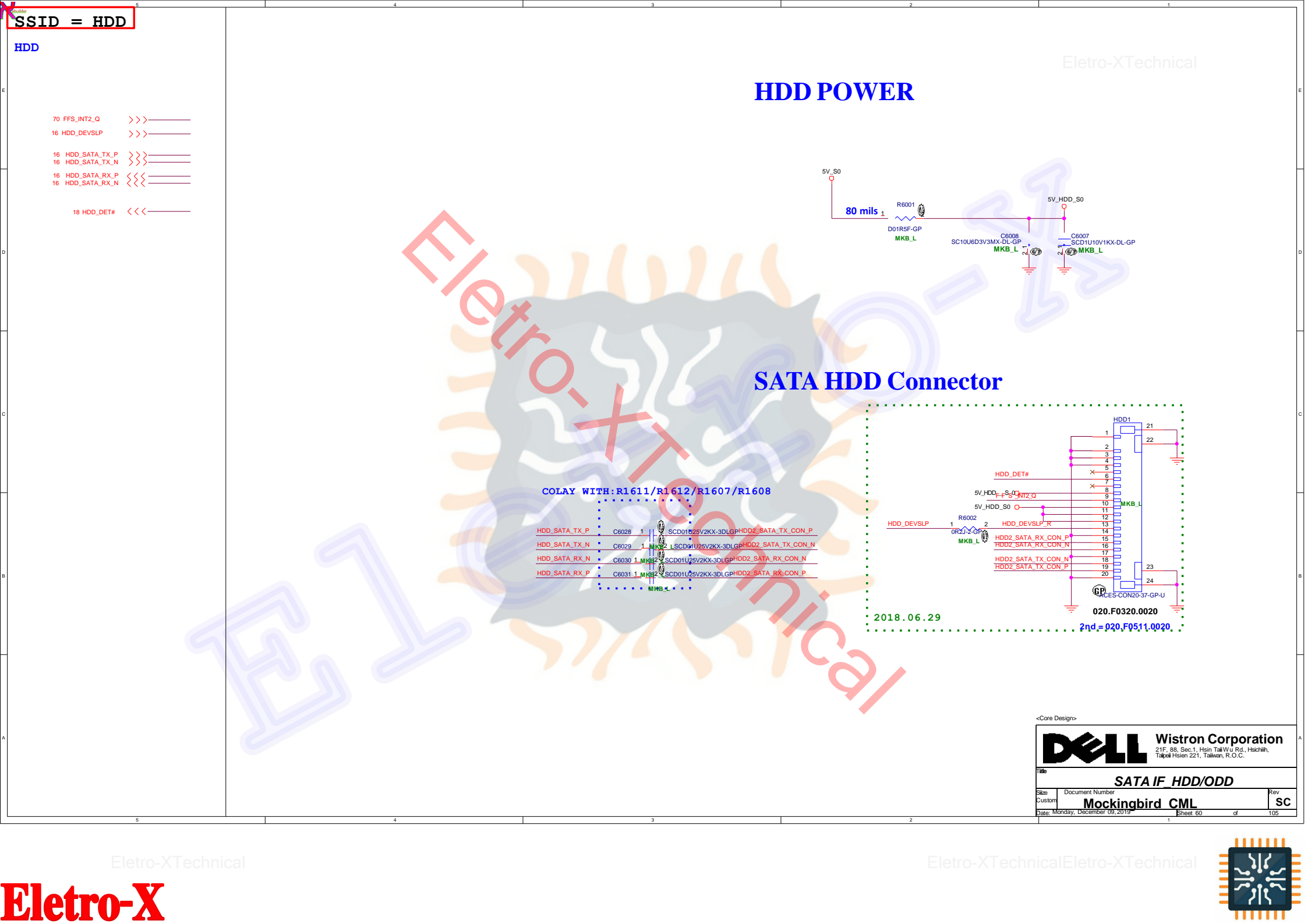
## HDMI CONN



<Core Design>

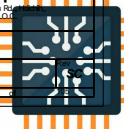
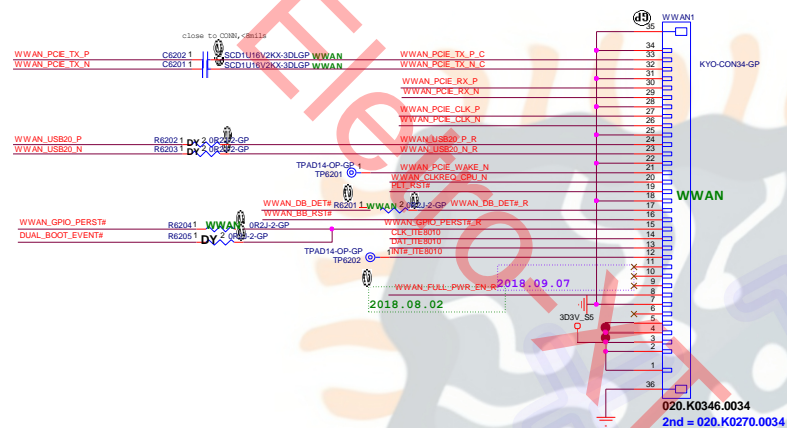
<b>DELL</b>		<b>Wistron Corporation</b>	
21F, 88, Sec.1, HsinTaiWu Rd., Hsichin, Taipei-Hsien 221, Taiwan, R.O.C.			
HDMI		Rev SC	
Size Custom	Document Number	Mockingbird_CML	
Date: Monday, December 09, 2019	Sheet 57	of 105	







Date: Monday, December 09, 2019 Sheet 61





SSID = Power BTN

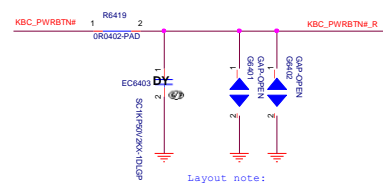
Power button

Eletro-XTechnical

24 KBC\_PWRBTN# <<< \_\_\_\_\_  
66 KBC\_PWRBTN\_R <<< \_\_\_\_\_



0614 Layout HT

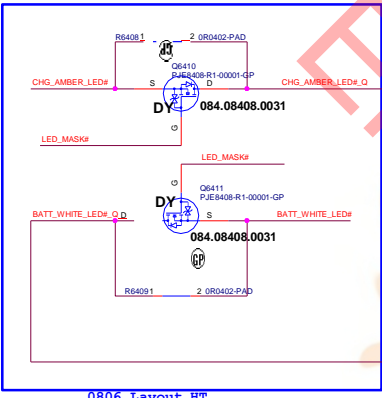


Layout note:  
G6401 place to bottom  
G6402 place to top

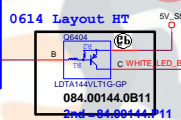
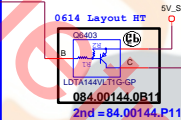
SSID = Battery LED

Low activated from KBC GPIO

24,66 LED\_MASK# >>> \_\_\_\_\_  
24 CHG\_AMBER\_LED# >>> \_\_\_\_\_  
24 BATT\_WHITE\_LED# >>> \_\_\_\_\_



0806 Layout HT



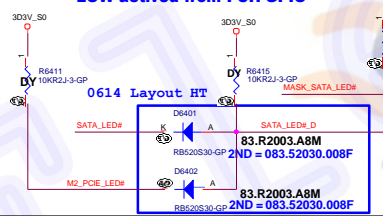
Battery LED1 (AMBER\_LED)

Battery LED2 (WHITE\_LED)

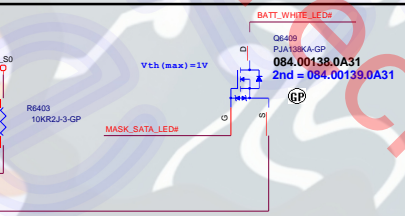
SSID = HDD LED

SATA HDD LED  
LOW activated from PCH GPIO

24 MASK\_SATA\_LED# >>> \_\_\_\_\_  
16 SATA\_LED# >>> \_\_\_\_\_  
63 M2\_PCH\_LED# <<< \_\_\_\_\_

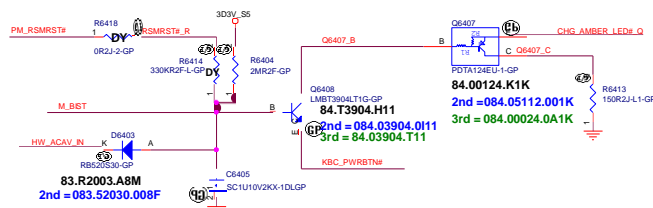


0614 Layout HT



SSID = M-BIST

17 PM\_RSMRST# >>> \_\_\_\_\_  
24 M\_BIST >>> \_\_\_\_\_  
24,44 HW\_ACAV\_IN >>> \_\_\_\_\_



BOLT 15 32bit/0822

**Wistron Corporation**  
2/F, Bldg. No. 1, Hsinchu WU Rd., Hsinchu,  
Taipei 30501, Taiwan, R.O.C.

**LED Board&Power Button**

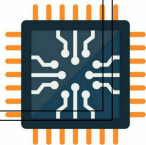
Size	Document Number	Rev
A2	Mockingbird_CML	SC

File: Mockingbird\_CML Date: 01/10/2019 Page: 64 of 105

Eletro-XTechnical

Eletro-XTechnical Eletro-XTechnical

Eletro-X

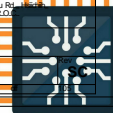






# Eletro-X

Wistron Confidential document, Anyone can not  
Duplicate, Modify, Forward or any other purpose  
application without get Wistron permission



SSID = Debug

ESPI

18,24 ESPI\_CLK >>> \_\_\_\_\_  
18,24 ESPI\_RESET# >>> \_\_\_\_\_  
18,24 ESPI\_CS# >>> \_\_\_\_\_

18,24 ESPI\_IO[3..0] <<>> \_\_\_\_\_  
ESPI\_IO3  
ESPI\_IO2  
ESPI\_IO1  
ESPI\_IO0

UART

24 HOST\_DEBUG\_TX >>> \_\_\_\_\_  
20 UART\_2\_CTXD\_DRXD >>> \_\_\_\_\_  
20 UART\_2\_CRXD\_DTXD <<< \_\_\_\_\_

Eletro-XTechnical

ESPI Debug Connector

Eletro-XTechnical

3D3V\_S0

HOST\_DEBUG\_TX R6801 1 DV 0R1J-GP HOST\_DEBUG\_TX\_CON  
UART\_2\_CTXD\_DRXD R6802 1 DEBUG 0R1J-GP UART\_2\_CTXD\_DRXD\_CON  
UART\_2\_CRXD\_DTXD R6803 1 DEBUG 0R1J-GP UART\_2\_CRXD\_DTXD\_CON  
ESPI\_CLK TPAD14-OP-GP 1 TP6801  
ESPI\_RESET# TPAD14-OP-GP 1 TP6802  
ESPI\_CS# TPAD14-OP-1GP TP6803  
ESPI\_IO3 TPAD14-OP-1GP TP6804  
ESPI\_IO2 TPAD14-OP-1GP TP6805  
ESPI\_IO1 TPAD14-OP-1GP TP6806  
ESPI\_IO0 TPAD14-OP-1GP TP6807  
TPAD14-OP-1GP TP6808  
TPAD14-OP-GP TP6809  
TPAD14-OP-1GP TP6810  
TPAD14-OP-GP TP6811

<Core Design>



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

A4

Document Number

Mockingbird\_CML

Date: Monday, December 09, 2019

Sheet 68 of

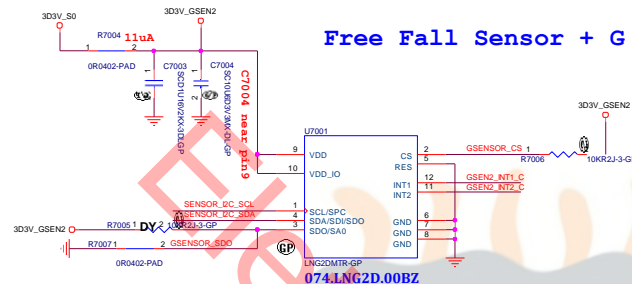


# Mantis Accelerometer for adaptive thermal and HDD protection

Eletro-XTechnical

The slave address (SAD) associated to the **LNG2DM** is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I<sup>2</sup>C lines.

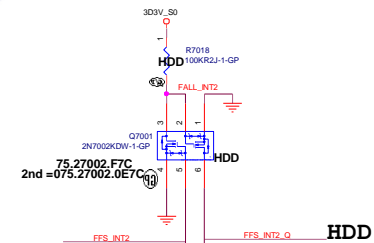
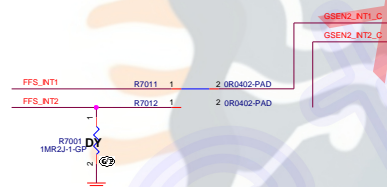
## Free Fall Sensor + G Sensor



Hellicat & MKB-L(8bit) :074.LNG2D.00BZ  
MKB-N/V(12bit) :074.LIS2D.M002

### Note:

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



### Note:

- (1) Keep all signals are the same trace width. (included VDD, GND).
- (2) No VIA under IC bottom.

Eletro-XTechnical

Eletro-XTechnical





SSID =TypeC

74 PD\_VBUS\_C\_CTRL1 <<< \_\_\_\_\_

EC

24 TYPEC\_SMBDA >>> \_\_\_\_\_

24 TYPEC\_SMBCLK >>> \_\_\_\_\_

74 VBUS\_P\_CTRL <<< \_\_\_\_\_

24 CCG5\_IC\_INT# >>> \_\_\_\_\_

0513

MUX TU5B546

73 IC\_DATA\_PD >>> \_\_\_\_\_

73 IC\_CLK\_PD >>> \_\_\_\_\_

4.73 DP1\_HPD\_CPU <<< \_\_\_\_\_

73 CCG5\_SBU1 <<< \_\_\_\_\_

73 CCG5\_SBU2 <<< \_\_\_\_\_

74 NX5P3363\_FO >>> \_\_\_\_\_

TYPE-C CONNECTOR

73 USB1\_CC1 >>> \_\_\_\_\_

73 USB1\_CC2 >>> \_\_\_\_\_

73 TOP\_MUX\_P\_L >>> \_\_\_\_\_

73 TOP\_MUX\_N\_L >>> \_\_\_\_\_

73 BOT\_MUX\_P\_L >>> \_\_\_\_\_

73 BOT\_MUX\_N\_L >>> \_\_\_\_\_

73 USB1\_SBU1 <<< \_\_\_\_\_

73 USB1\_SBU2 <<< \_\_\_\_\_

PCH

16 USB4\_USB20\_P >>> \_\_\_\_\_

16 USB4\_USB20\_N >>> \_\_\_\_\_

From System

303V\_S5

D7202

SBA0520Q-R1-00001

083.00520.0F8F

2nd=083.05S40.001F

VCC3PD\_1

303V\_S5

D7203

SBA0520Q-R1-00001

083.00520.0F8F

2nd=083.05S40.001F

VCC3PD

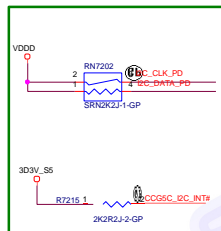
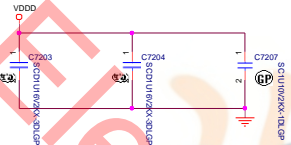
For debattery

1 R7210

2 VDDO

0R0402-PAD

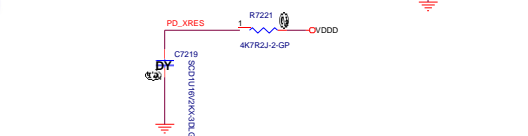
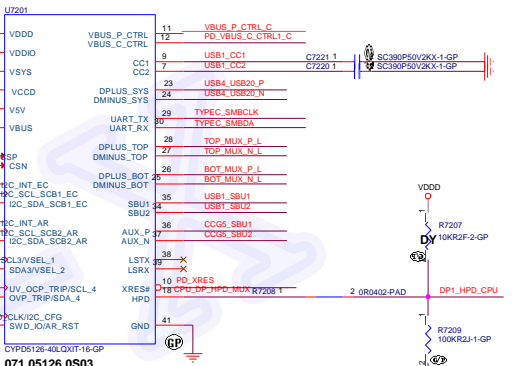
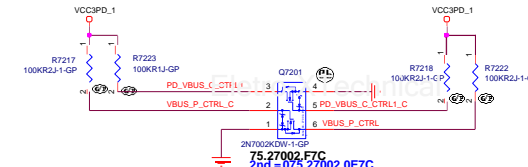
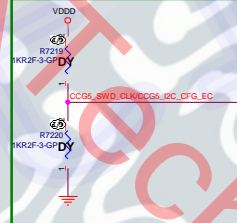
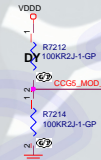
Power



MOD ID Settings



MOD ID Settings



<Core Design>



Wistron Corporation

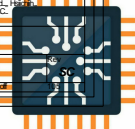
21F, 8B, Sec.1, HsinTaiWu Rd., HsinTaiWu, Tainan, R.O.C.

USB PD(CYPD5126)

Mockingbird\_CML

Date: Monday, December 03, 2019

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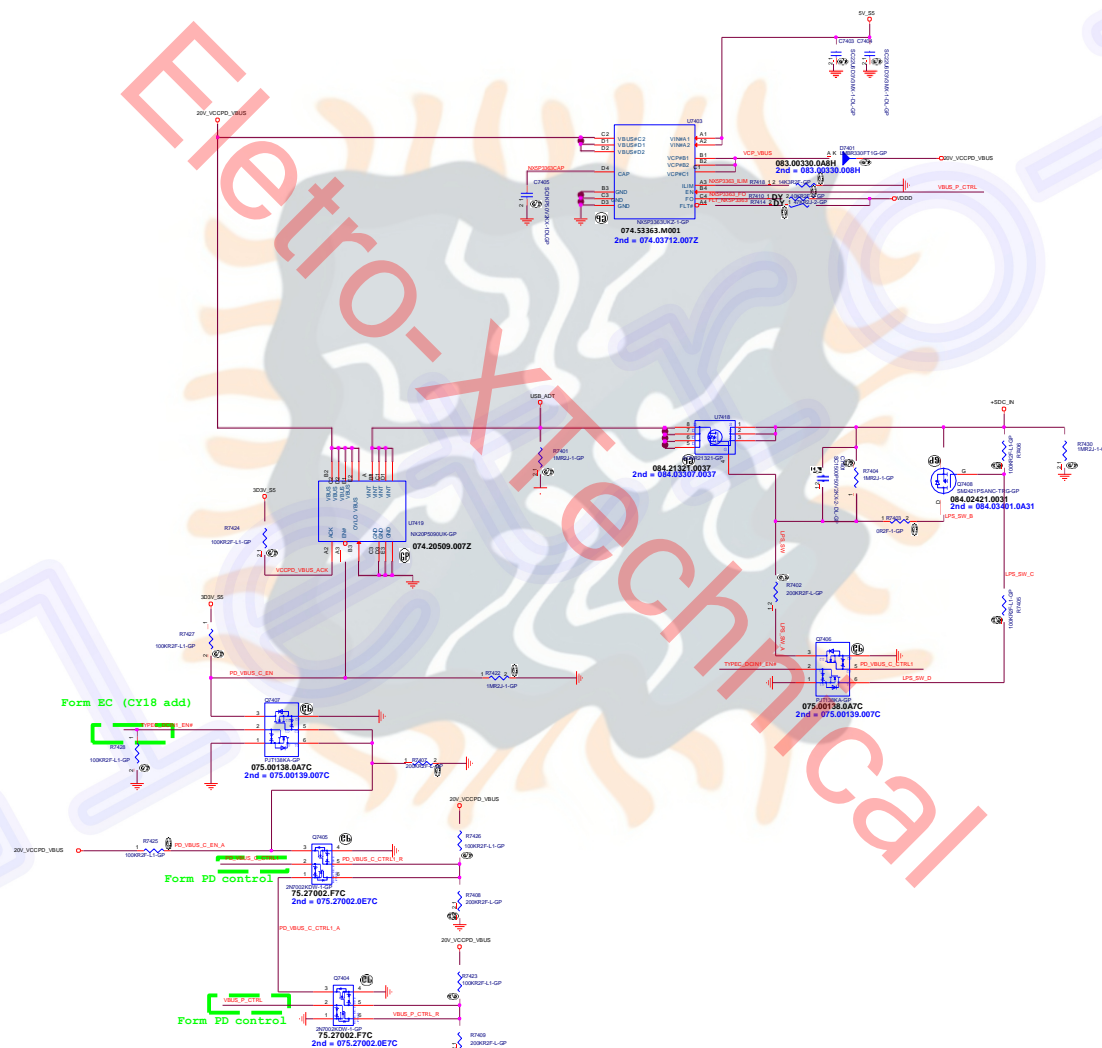


Eleto-X

Eleto-XTechnical

Eleto-XTechnical





# SSID = TPM

17,40,61,62,63,66 PLT\_RST# >>> \_\_\_\_\_

18,24,25 SPI\_CLK\_ROM >>> \_\_\_\_\_

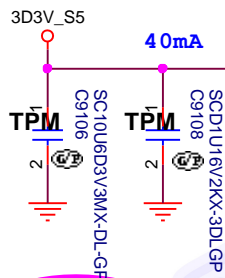
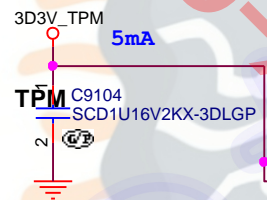
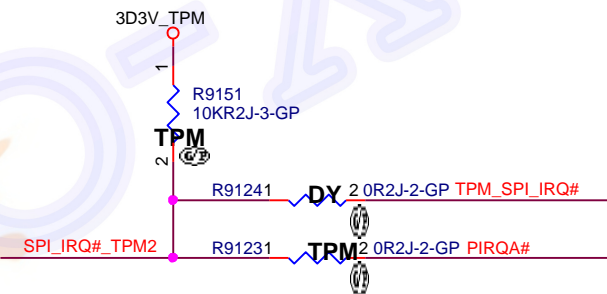
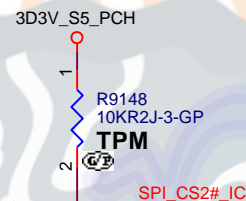
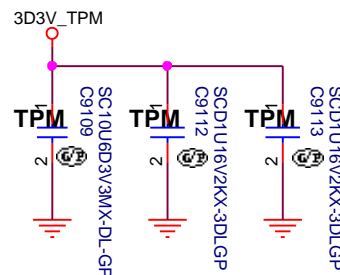
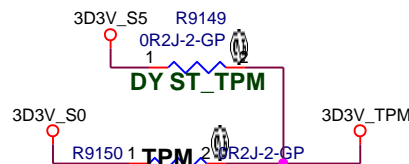
15,18,24,25 SPI\_SI\_ROM >>> \_\_\_\_\_

18,24,25 SPI\_SO\_ROM >>> \_\_\_\_\_

18 SPI\_CS\_ROM\_N2 >>> \_\_\_\_\_

20 PIRQA# >>> \_\_\_\_\_

18 TPM\_SPI\_IRQ# >>> \_\_\_\_\_



SPI\_SI\_ROM R9133 1 TPM 15R1F-GP SPI\_SI\_ROM TPM 21

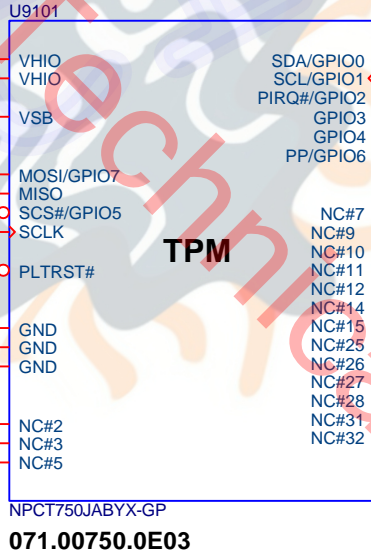
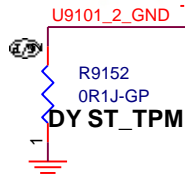
SPI\_SO\_ROM R9132 1 TPM 15R1F-GP SPI\_SO\_ROM TPM 24

SPI\_CS\_ROM\_N2 R9130 1 TPM 0R1J-GP SPI\_CS2#\_IC

SPI\_CLK\_ROM R9138 1 TPM 15R1F-GP SPI\_CLK\_ROM TPM 19

Close to U2501

PLT\_RST#



29 TPM\_GPIO0 1 TP9101

30 TPM\_GPIO1 1 TP9102

18 SPI\_IRQ#\_TPM2 1 TP9103

6 TPM\_GPIO3 1 TP9104

13 TPM\_GPIO4 R9118 1 2K2R1F-GP SPI\_CS\_ROM\_N2

4 TPM\_GPIO6\_PP 1 TP9104

NC#7

NC#9

NC#10

NC#11

NC#12

NC#14

NC#15

NC#25

NC#26

NC#27

NC#28

NC#31

NC#32

<Core Design>

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (TPM)**

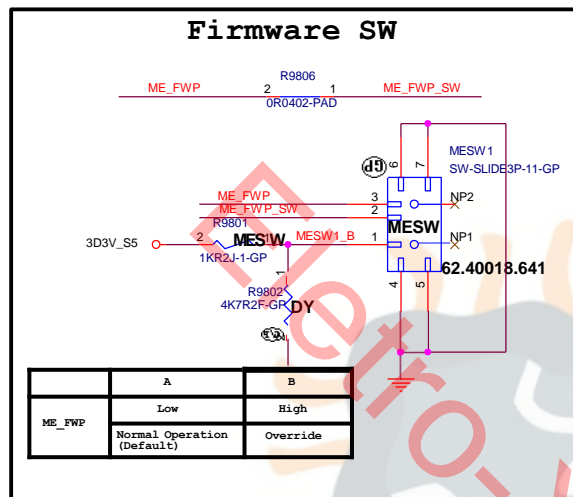
Size A4 Document Number **Mockingbird\_CML**

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Main Func = Firmware SW

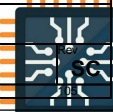
19 ME\_FWP\_SW >>> \_\_\_\_\_  
24 ME\_FWP <<< \_\_\_\_\_



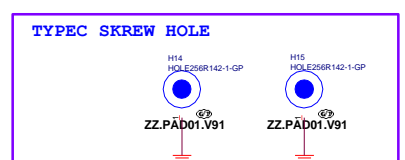
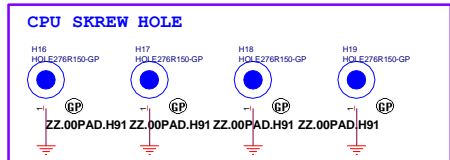
	3	1
ME_FWP	LOW	HIGH
	Normal Operation (Default)	Override

<Core Design>

<b>DELL</b>		<b>Wistron Corporation</b>	
		21F, 88, Sec.1, HsinTaiWu Rd., Hsichih, Taipei-Hsien 221, Taiwan, R.O.C.	
Title		CRT Switch	
Size A3	Document Number		
Date: Monday, December 09, 2019		Sheet 98 of 98	



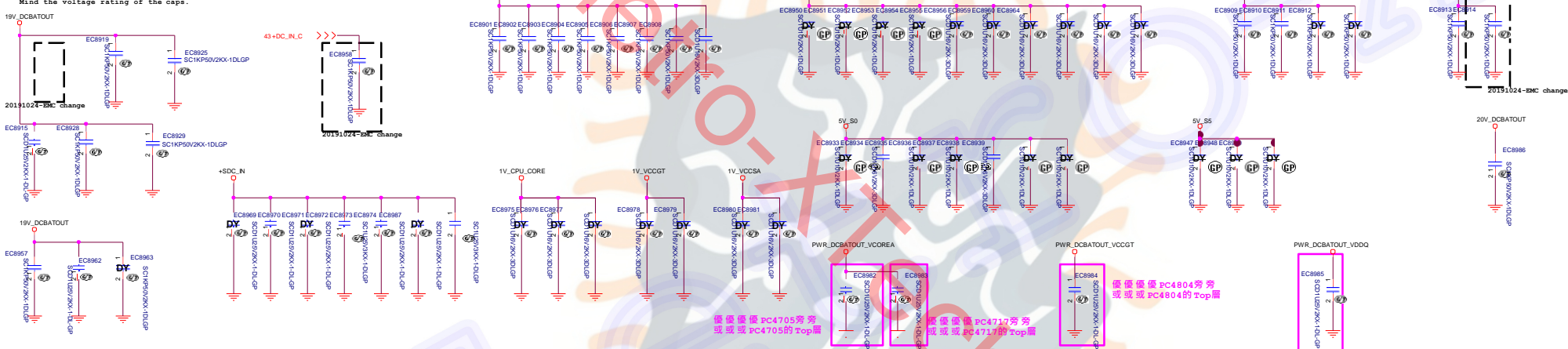
# SSID = UnusedParts



Eletro-XTechnical

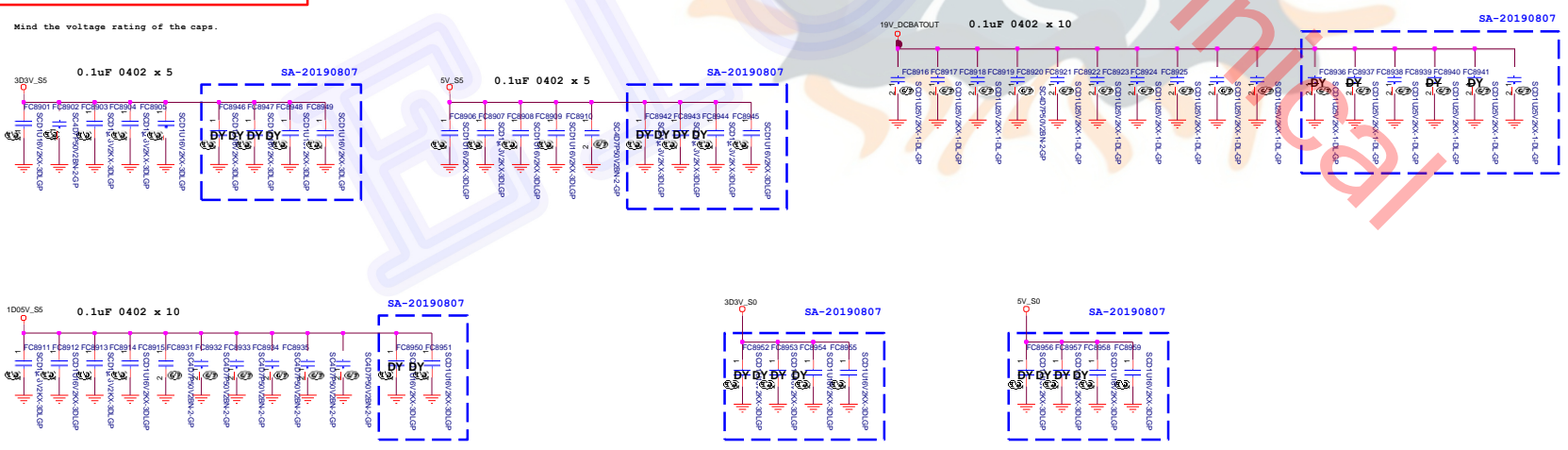
# SSID = EMI Capacitors

Mind the voltage rating of the caps.



# SSID = RF Capacitors

Mind the voltage rating of the caps.



Eletro-XTechnical

Eletro-XTechnical

Eletro-X

Wistron Corporation

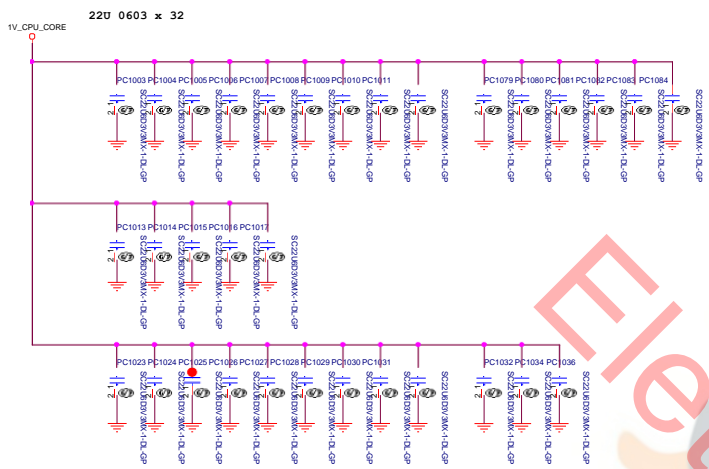
2F, 8A, Sec. 1, HsinTai Wu Rd., HsinTai Wu, Taipei 105, Taiwan, R.O.C.

UNUSED PARTS/EMI Capacitors

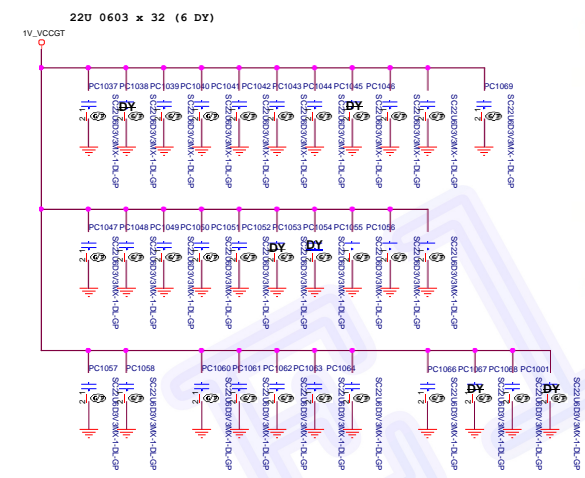
Mockingbird CML

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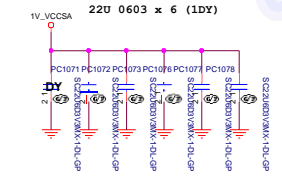
1V\_CPU\_CORE



VCCGT



VCCSA



Whiskey Lake U 4+2 Bulk Decoupling Example

Bulk Decoupling Locations	Example	Notes
VCCORE Power Plane at VR output	4x 220uF (@4.5mO ESR)	Placed at primary side near to VR output
VCCGT Power Plane at VR output	2x 220uF (@4.5mO ESR)	Placed at primary side near to VR output

Notes:

- These examples are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.
- Bulk decoupling is not a "requirement" but recommendation only. It is an example of VR design/VR bandwidth. Customer should work with respective vendor to validate their VR & bulk decoupling designs to ensure the electrical requirements are met.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 1 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402		Place as close to the package as possible
	18x 47uF 0805 (6.3V)		Place as close to the package as possible. Can be placed on as either Primary or back side cap.

Decoupling Requirements for Whiskey Lake U 4+2 Processor (Sheet 2 of 2)

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCGT	15x 22uF 0603		Place underneath the package
	4x 47uF 0805 (6.3V)		
		11x 1uF 0402/0201	Place as close to the package as possible
		15x 10uF 0402	
VCCSA		4x 0402	Placeholder only.
	6x 10uF 0402	7x 10uF 0402	
	2x 47uF 0805 (6.3V)		
	2x 0805		Placeholder Only
VDDQ		4x 1uF 0402/0201	Place as close to the package as possible.
		3x 10uF 0402	
	1x 22uF 0603		
	6x 10uF 0402		
VCCIO	4x 1uF 0201		Place underneath the package
	6x 10uF 0402		Place as close to the package as possible
VCCPLL_OC	4x 0402		Placeholder Only
	1x 1uF 0402		Do not merge VCCPLL, VCCPLL_OC and VCCGT to any noisy and high current power rail and do not route them close/adjacent to and reference to, any noisy and high current rail on top and bottom layers - as this may impact to PLL failing to phase lock.
VCCPLL	1x 0.1uF 0201		Place as close as possible to BGA.
	1x 1uF 0402		Place as close as possible to BGA and can be placed on as either Primary or backside cap.
	1x 0805		Placeholder Only.
			Can be placed on as either Primary or back side cap.
VCCGT	1x 1uF 0402		
VCCSA	1x 1uF 0402		

Notes:

- The 6.3V voltage is for the higher capacitance retention; more 0805 components will be required for a lower voltage capacitor rating. Assumption: VR loop bandwidth ~ 250kHz e.g., 1MHz switching VR
- Component placement order: Package edge > 0402 caps > 0603 caps > 0805 caps > Bulk caps > Power source.

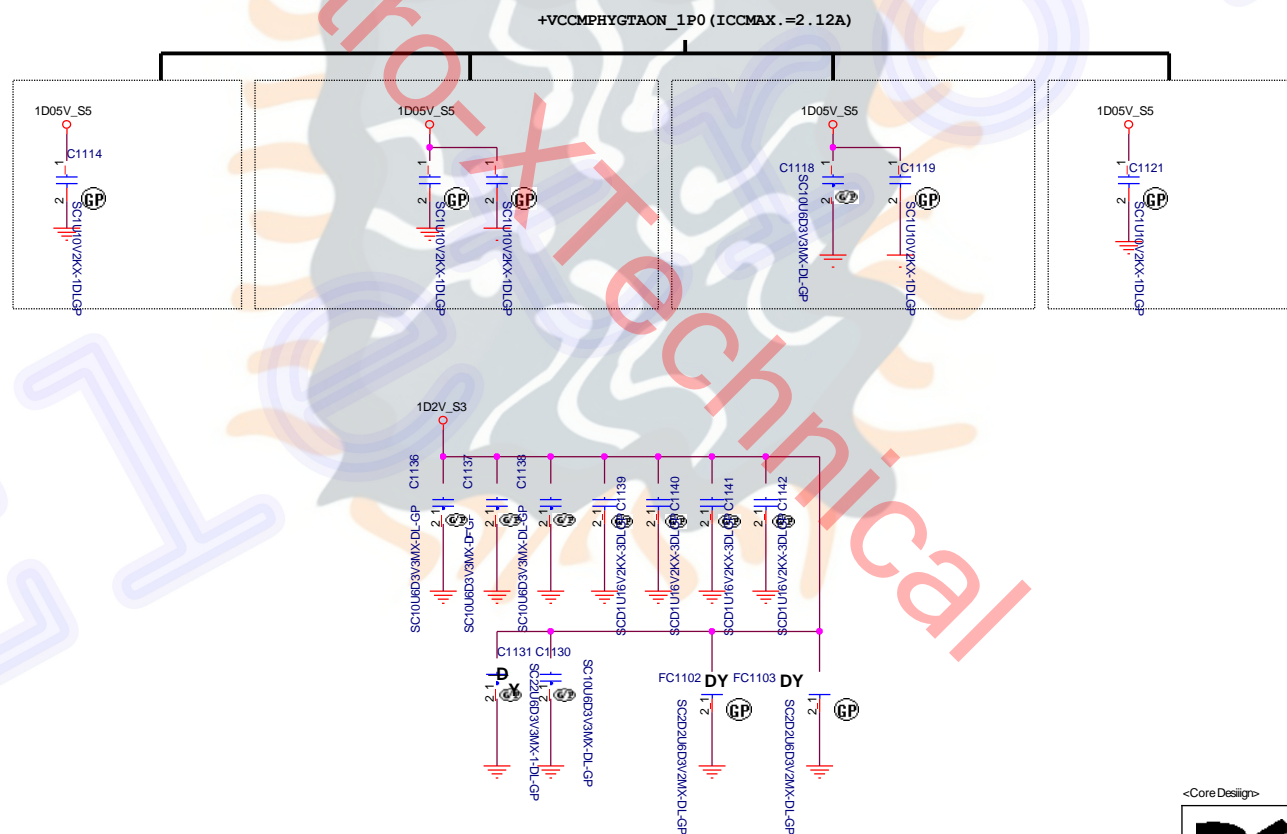
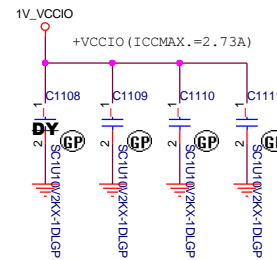
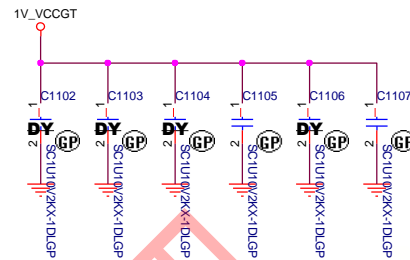
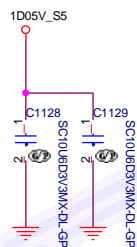
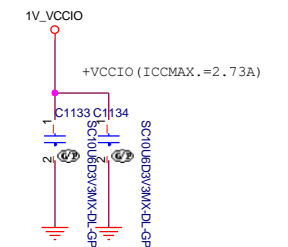
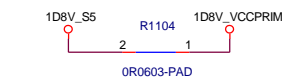
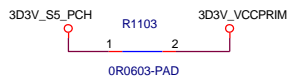
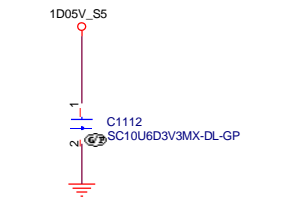
SSID = CPU

## PCH DERIVED RAILS

## UNSLICED GT

## VCCIO

Eletro-XTechnical



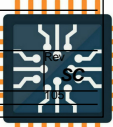
**Layout Note:**  
1uF:  
C1174 near N15  
C1180 near K15  
C1173 near AF20  
C1172 near N18  
C1175 near AB19  
22uF :  
C1182 C1184 near N15  
10uF:  
C1176 near N15

U-line 23e 28W  
IccMax current-10ms max = 34 A

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, HsinTaiWu Rd., Hsichih,  
Taippei-Hsien 221, Taiwan, R.O.C.

Title: CPU (Power CAP?)  
Size: A3 Document Number  
Date: Monday, December 09, 2019 Sheet 11 of 11







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[ROW Only] PHYSICAL_ACCESS_ENABLED (SPE PROTECT)	
CFG[1]	0 = DISABLED SET OFX ENABLED SET IN CORE INTERFACE W0R
	1 = SET ACCESS

PCH strappin:



(H43016)	
DISPLAY PORT PROBLEM CRAP	
QPC[4]	<p>1 - Unable</p> <p>In external Display Port device is connected to the Embedded Display Port.</p> <p>2 - Embedded interface</p> <p>In Physical Display Port attached to Embedded DisplayPort*. No connect for display.</p>



